



Specification for 4.2 inch EPD

Model NO. : OKRA0420RWS830F0

OKRA's Confirmation:

Prepared by	Checked by	Approved by

Customer approval:

Customer	Approved by	Date



Revision History

Version	Content	Date	Producer
2.0	New release	2020/11/11	



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1. Over View

OKRA420RWS830F0 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 4.2inch active area contains 300×400 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆ 300×400 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor



3.Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	DPI:120
Active Area	84.8×63.6	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Rectangle		
Outline Dimension	91 (H)×77 (V) ×1.2(D)	mm	
Weight	16.1±0.3	g	

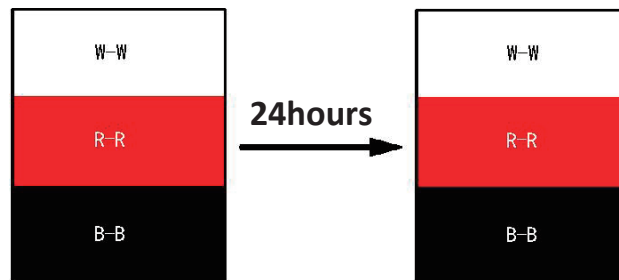
Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value		-	13	15		3-1
	Black State A* value		-	4	6		3-1
	Black Ghosting ΔE		-	2	-		3-1
	After 24hour colour changed		-	2	-		3-4
WS	White State L* value		62	65	-		3-1
	White State A* value		-	0	1		3-1
	White Ghosting ΔE		-	2	-		3-1
	After 24hour colour changed		-	2	-		3-4
RS	Red State L* value		27	28	32		3-1
	Red State A* value		36	40	45		3-1
	Red Ghosting ΔE		-	3	-		3-1
	After 24hour colour changed		-	2	-		3-4
T update	Image update time	at 23 °C	-	17	-	sec	
R	White Reflectivity	White	30	34	-	%	3-1
CR	Contrast Ratio	Indoor	15:1	20:1	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

3-4. After 24hour Colour Changed:



W: Max $\Delta E(W-W) < 2$, K: Max $\Delta E(B-B) < 2$, R: Max $\Delta Eab(R-R) < 2$.



4.Mechanical Drawing of EPD Module

Confirmation:	DATE 2020-06-24	REV. A	MODIFICATION FIRST ISSUE
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FRONT VIEW

SIDE VIEW

BACK VIEW

NOTE

- 1 DISPLAY MODULE 4.2" ARRAY FOR EPD
- 2 DRIVER IC:SSD1683
- 3 RESOLUTION:300gateX400source
- 4 PIXEL SIZE:0.212mmX0.212mm

TOLERANCES UNMARKED

ANGLES ± 5°

.X = ± 0.4mm

.XX = ± 0.20mm

.XXX = ± 0.20mm

TITLE: EPD

PROJECT: OKRA0420RWS830F0

REV: A

DATE: 20.06.24

CUST. P/N:

DWN: NN ZHAO

CHK: CC ZHENG

APPR: XF NIE

UNIT: mm

3RD ANGLE:

PAGE: 1/1



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin,I /O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin



Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +6.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOU	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to+40	°C.
Optimal Storage Temp	TSTGo	23±3	°C.
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. We guarantee the single pixel display quality for 0-35°C, but we only guarantee the barcode readable for 35-40°C.
3. The storage time is within 10 days for -25°C ~ 0°C or 40°C ~ 60°C.
The display screen should be kept white and face up.

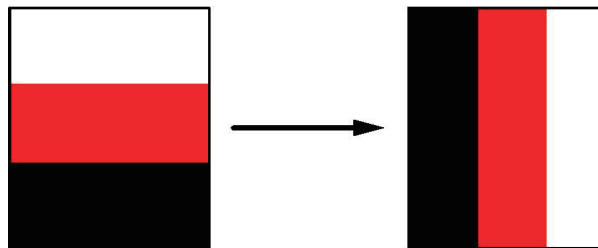


6.2 Panel DC Characteristics

The following specifications apply for: $V_{SS}=0V$, $V_{CI}=3.0V$, $TOPR = 23^{\circ}C$.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	V_{CI}	2.2	3.0	3.7	V
Core logic voltage	V_{DD}		V_{DD}	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	$0.8 V_{CI}$	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	$0.2 V_{CI}$	V
High level output voltage	V_{OH}	$I_{OH} = -100\mu A$	-	$0.9 V_{CI}$	-	-	V
Low level output voltage	V_{OL}	$I_{OL} = 100\mu A$	-	-	-	$0.1 V_{CI}$	V
Typical power	P_{TYP}	$V_{CI}=3.0V$	-	-	18.4		mW
Deep sleep mode	P_{STPY}	$V_{CI}=3.0V$	-	-	0.003	-	mW
Typical operating current	I_{opr_VCI}	$V_{CI}=3.0V$	-	-	6.2	-	mA
Image update time	-	$23^{\circ}C$	-	-	17	-	sec
Typical peak current	I_{opr_VCI}	$2.2\sim 3.7V$			50	60	mA
Sleep mode current	I_{slp_VCI}	DC/DC off No clock No input load Ram data retain	-	-	20		μA
Deep sleep mode current	I_{dslp_VCI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	μA

Notes: 1. The typical power is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern.



- The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OKRA.
- Electrical measurement: Tektronix oscilloscope - MDO3024,
Tektronix current probe - TCP0030A.



6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	TBD	-	V
Positive Source output voltage	V _{SH}	-	S ₀ ~S ₃₉₉	+14.5	+15	+15.5	V
Negative Source output voltage	V _{SL}	-	S ₀ ~S ₃₉₉	-15.5	-15	-14.5	V
Positive gate output voltage	V _{gh}	-	G ₀ ~G ₂₉₉	+21	+22	+23	V
Negative gate output voltage	V _{gl}	-	G ₀ ~G ₂₉₉	-21	-20	-19	V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

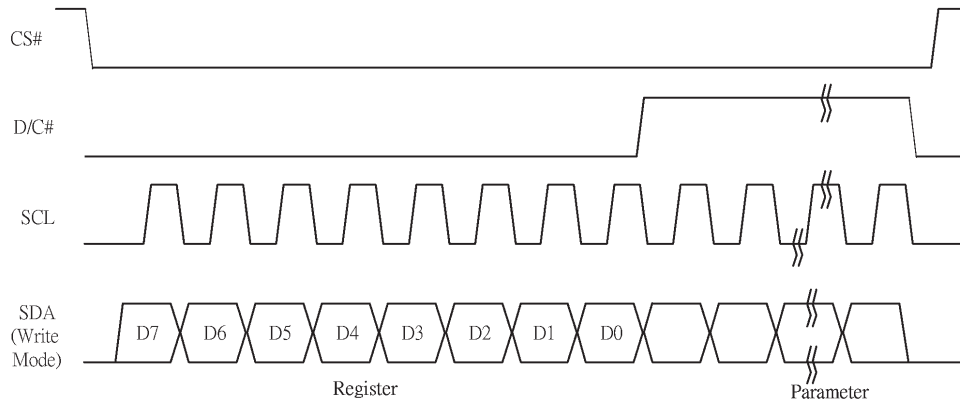
Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.



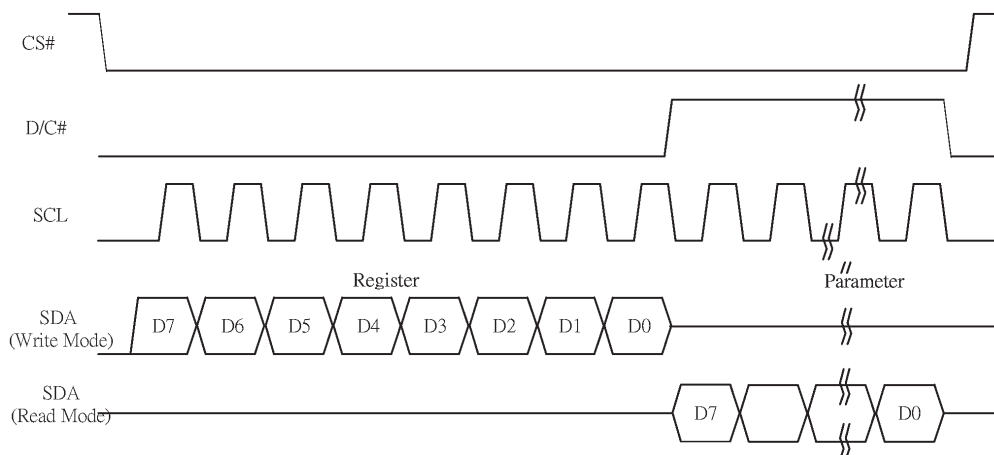
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode





6.4.3 MCU Serial Interface (3-wire SPI)

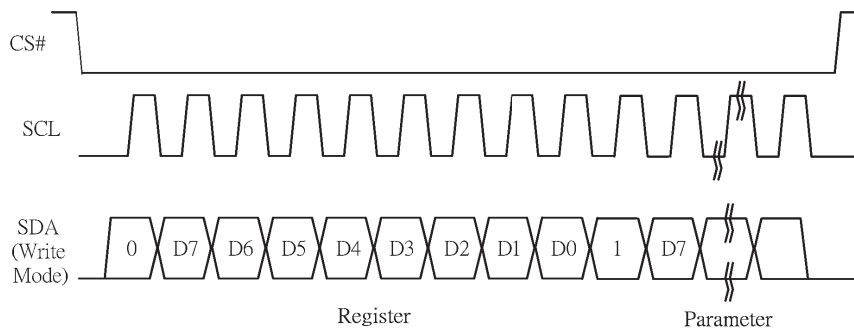
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

Figure 6-3: Write procedure in 3-wire SPI mode

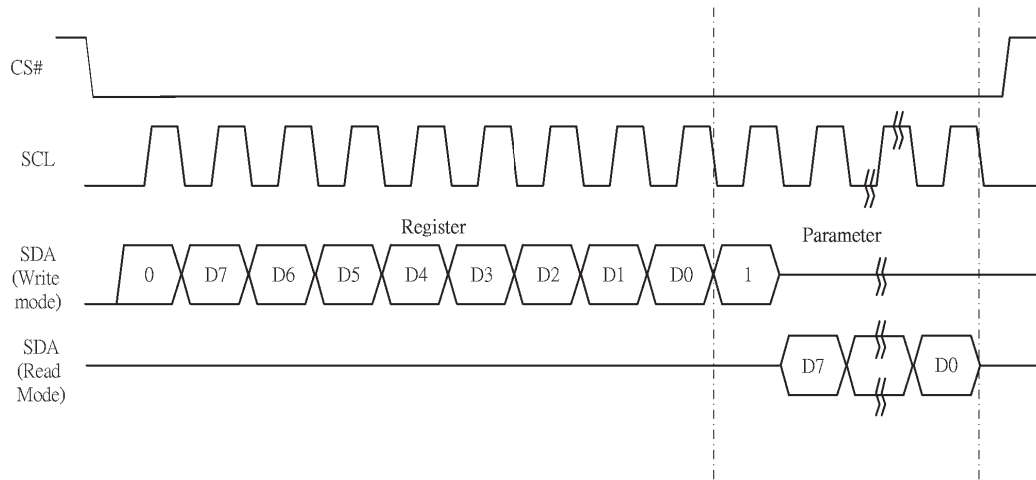


In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

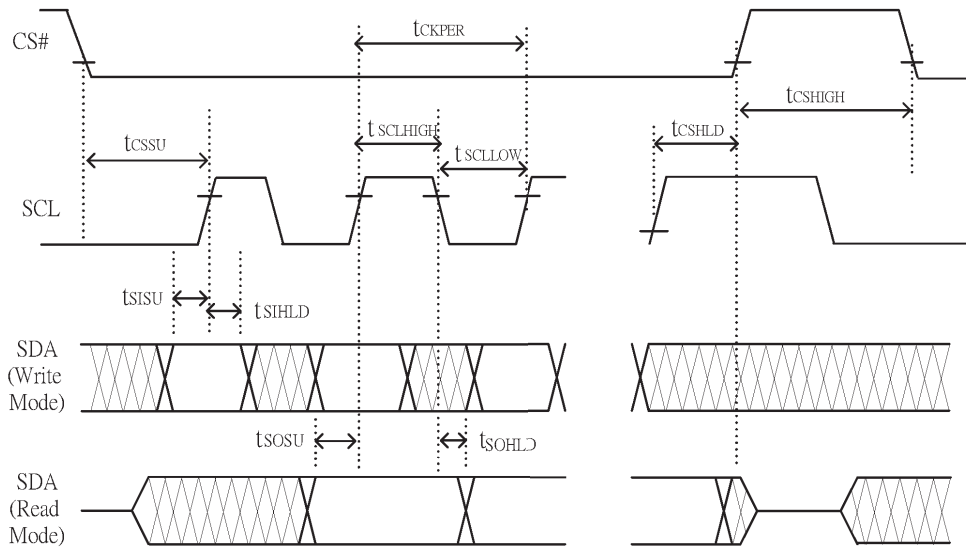


Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.



Changed Diagram

**Serial Interface Timing Characteristics**

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

**7.Command Table**

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[8:0]=012Bh Set B[8:0]=00h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	Set Gate Driving voltage A[4:0]=17h[POR],VGH at 20V[POR] VGH setting from 10V to 21V
0	1		0	0	0	A4	A3	A2	A1	A0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	Set Source Driving voltage A[7:0]= 41h[POR],VSH1 at 15V B[7:0]=A Ch[POR],VSH2 at 5.4V C[7:0]= 32h[POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		



0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																																																						
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																																								
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																								
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																																								
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<table border="1"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Selection</th> <th>Strength</th> </tr> </thead> <tbody> <tr><td>000</td><td>1(Weakest)</td><td></td></tr> <tr><td>001</td><td>2</td><td></td></tr> <tr><td>010</td><td>3</td><td></td></tr> <tr><td>011</td><td>4</td><td></td></tr> <tr><td>100</td><td>5</td><td></td></tr> <tr><td>101</td><td>6</td><td></td></tr> <tr><td>110</td><td>7</td><td></td></tr> <tr><td>111</td><td>8(Strongest)</td><td></td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Bit[3:0]</th> <th>Min Off Time Setting of GDR [Time unit]</th> </tr> </thead> <tbody> <tr><td>0000 ~ 0011</td><td>NA</td></tr> <tr><td>0100</td><td>2.6</td></tr> <tr><td>0101</td><td>3.2</td></tr> <tr><td>0110</td><td>3.9</td></tr> <tr><td>0111</td><td>4.6</td></tr> <tr><td>1000</td><td>5.4</td></tr> <tr><td>1001</td><td>6.3</td></tr> <tr><td>1010</td><td>7.3</td></tr> <tr><td>1011</td><td>8.4</td></tr> <tr><td>1100</td><td>9.8</td></tr> <tr><td>1101</td><td>11.5</td></tr> <tr><td>1110</td><td>13.8</td></tr> <tr><td>1111</td><td>16.5</td></tr> </tbody> </table> D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1												Bit[6:4]	Driving Selection	Strength	000	1(Weakest)		001	2		010	3		011	4		100	5		101	6		110	7		111	8(Strongest)		Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000 ~ 0011	NA	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
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10	30ms																																																																	
11	40ms																																																																	



0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control	
0	1		0	0	0	0	0	0	0	A ₀			
												A[0] :	Description
												0	Normal Mode [POR]
												1	Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.	
0	1		0	0	0	0	0	A ₂	A ₁	A ₀			
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.	
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor	
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]	
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			
0	1		B ₇	B ₆	B ₅	B ₄	0	0	0	0			
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.	
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update BW RAM option A[7:4]=0100 (For BW) A[3:0]=0000[POR] Normal A[3:0]=0100	
0	1		0	0	0	0	A ₃	A ₂	A ₁	A ₀			



0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation Setting for LUT from MCU Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY C7 Then Disable Analog Then Disable OSC Setting for LUT from OTP according to external Temperature Sensor operation Then Enable Analog Then Load LUT 90 Enable Analog Then PATTERN DISPLAY 47 Then Disable Analog Then Disable OSC
	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this Command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=4Bh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~ B[7:0]: VCOM Information 3. C[7:0]~F[7:0]: Reserved 4. G[7:0]~H[7:0]: Module ID/ Waveform Version [2bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		



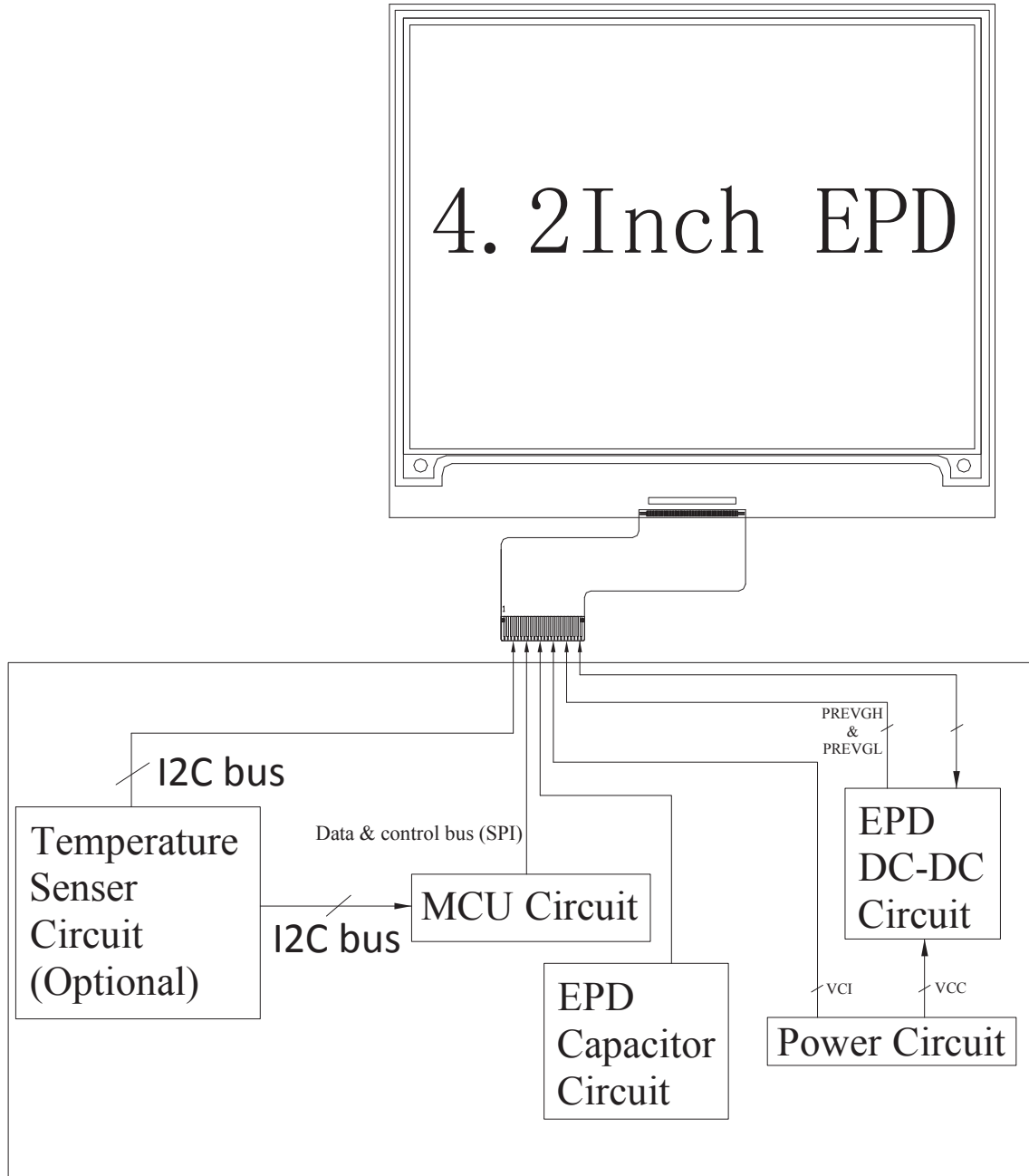
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1]
1	1		0	0	A5	A4	0	0	A1	A0		0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [70 bytes].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set A[6:0]=2Ch Default value will give 50Hz Frame frequency
0	1		0	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set A[3:0]=0Ah Default value will give 50Hz Frame frequency
0	1		0	0	0	0	A ₃	A ₂	A ₁	A ₀		



0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7:6] Select VBD		
0	1		A ₇	A ₆	A ₅	A ₄	0	0	A ₁	A ₀			A[7:6]	Select VBD as
													00[POR]	GS Transition Define A [1:0]
													01	Fix Level Define A [5:4]
													10	VCOM
													11	HIZ
													A [5:4] Fix Level Setting for VBD	
													A[5:4]	VBD level
													00[POR]	VSS
													01	VSH1
													10	VSL
													11	VSH2
													A[1:0]) BW Transition setting for VBD	
													A[1:0]	VBD Transition
											00 [POR]	LUT0		
											01	LUT1		
											10	LUT2		
											11	LUT3		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[5:0]: XSA[5:0], X Start, POR = 00h B[5:0]: XEA[5:0], X End, POR = 31h		
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀				
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], Y Start, POR = 012Bh B[8:0]: YEA[8:0], Y End, POR = 0000h		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	1		0	0	0	0	0	0	0	A ₈				
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀				
0	1		0	0	0	0	0	0	0	B ₈				
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: XAD[5:0], POR is 00h		
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 012Bh		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	1		0	0	0	0	0	0	0	A ₈				
0	0	74	0	1	1	1	0	1	0	0	Set Analog Block control	A[7:0] = 54h		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	0	7E	0	1	1	1	1	1	1	0	Set Digital Block control	A[7:0] = 3Bh		
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				

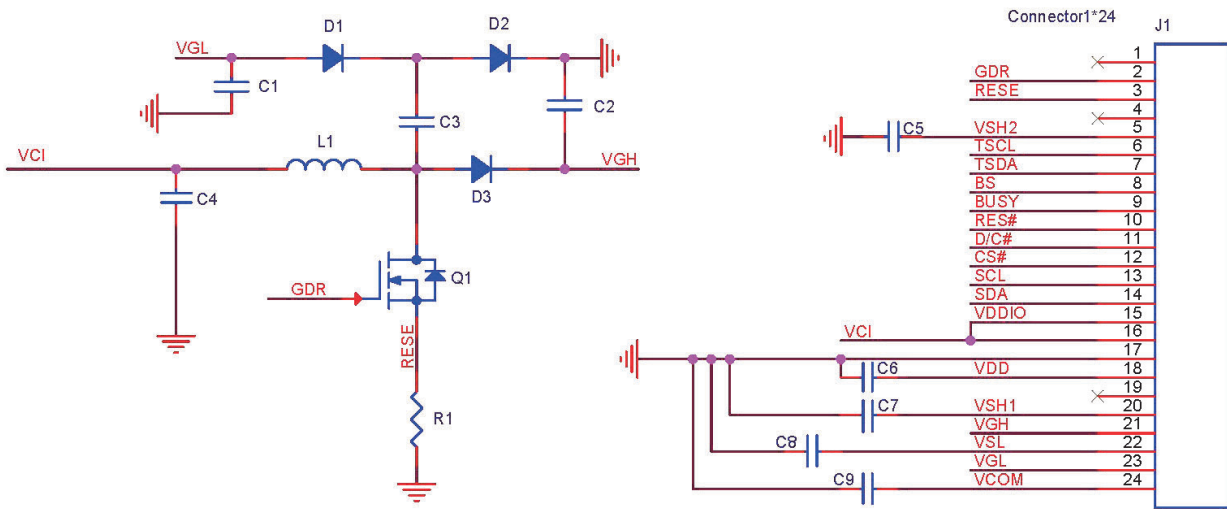


8. Block Diagram





9. Typical Application Circuit with SPI Interface

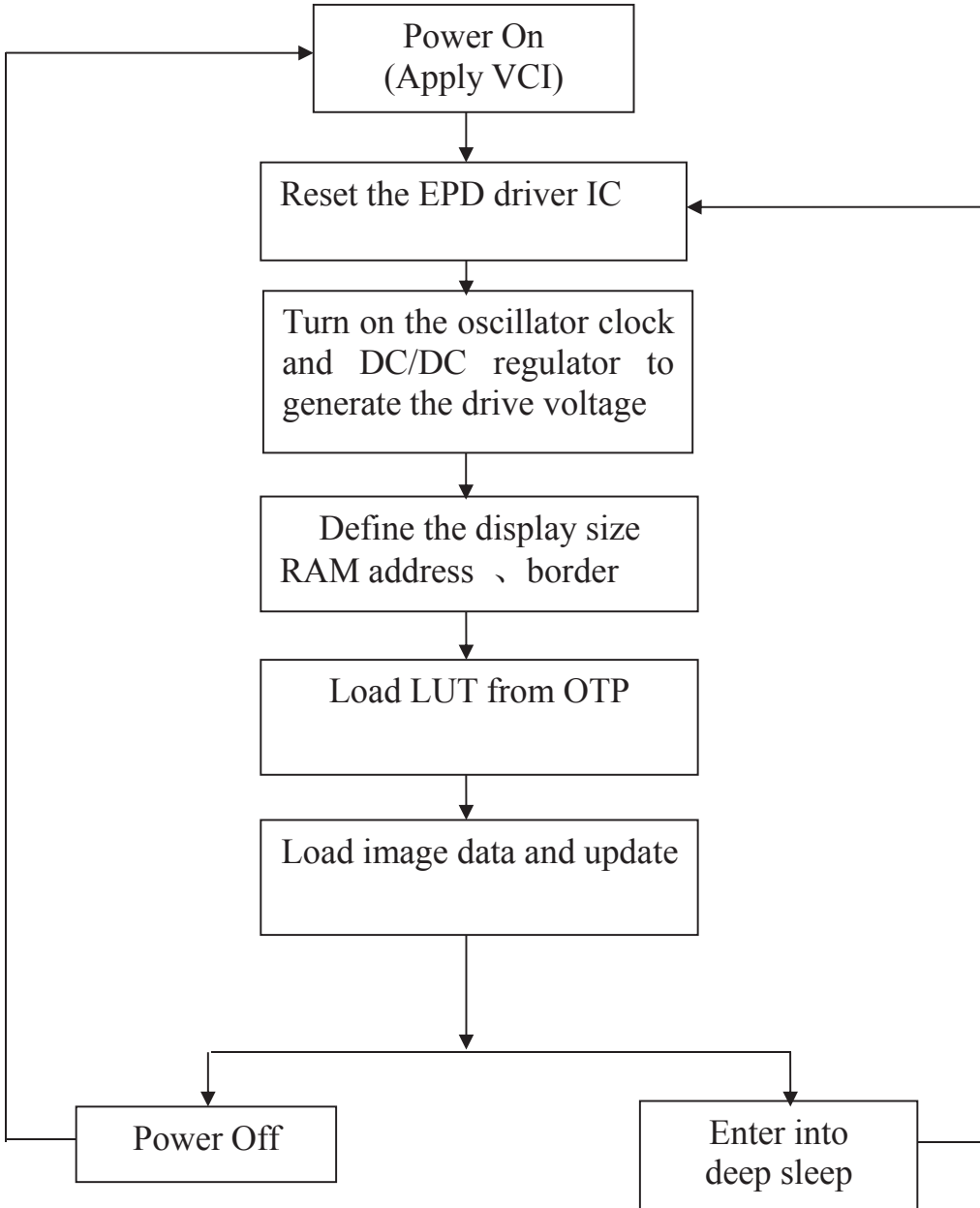


Part Name	Value	Reference Part	Requirements for spare part
C4 C6	1uF	0603;X5R/X7R;Voltage Rating:6v	
C1 C2 C3 C5 C7 C8	1uF	0805; X5R/X7R;Voltage Rating:25v	
C9	0.47uF	0805; X7R;Voltage Rating:25v	
R1	2.20hm	0805; 1%	
D4 D5 D6	Diode	MBR0530	
Q1	NMOS	Si1304BDL	
L2	47UH	CDRH2D18/LDNP-470NC	



10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow





10.2 LUT from OTP Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RES#	low	Hardware reset
delay	200us	
RES#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
SET VOLTAGE AND LOAD LUT		
LOAD IMAGE AND UPDATE		
Command 0x24	15000bytes	Load BW image (400/8*300)
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		



11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: 1. Stay white pattern for storage and non-operation test.

2. Operation is black→white-red pattern, the interval is 150s.

3. Put in 20°C--25°C for 1hour after test finished, The function ,appearance and display performance is OK.

12. Quality Assurance

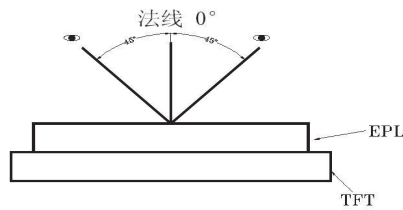
12.1 Environment

Temperature: 23±3°C
 Humidity: 55±10%RH

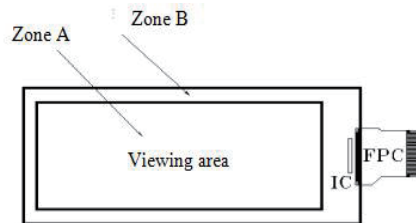
12.2 Illuminance

Brightness: 1200~1500LUX; distance: 20-30CM; Angle: Relate 45° surround.

12.3 Inspect method

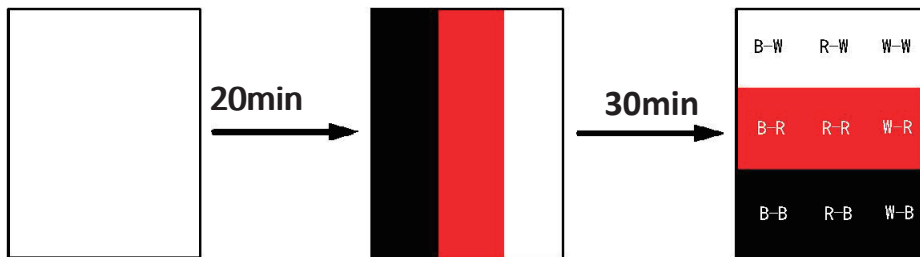


12.4 Display area



12.5 Ghosting test method

Three-color ghosting is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by OKRA.



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

W ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(W-W, R-W), \Delta E_{ab}(W-W, B-W), \Delta E_{ab}(B-W, R-W))$


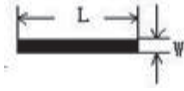
K ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(B-B, W-B), \Delta E_{ab}(B-B, R-B), \Delta E_{ab}(R-B, W-B))$

R ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(R-R, W-R), \Delta E_{ab}(R-R, B-R), \Delta E_{ab}(B-R, W-R))$



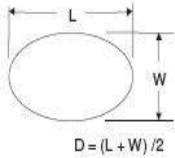
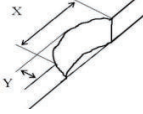
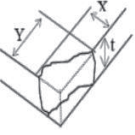
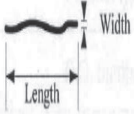

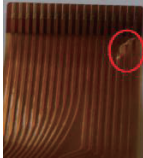
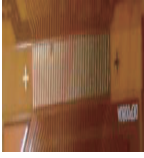
12.6 Inspection standard

12.6.1 Electric inspection standard

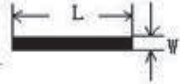
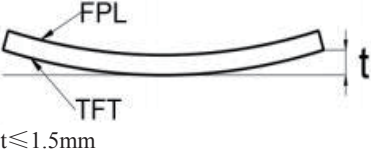
NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA		
2	Black/White spots	 $D \leq 0.3\text{mm}$, negligible $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$, Allowed $0.5\text{mm} < D$ Not Allow	MI	Visual inspection	Zone A
3	Black/White lines (No switch)	 $L \leq 1.0\text{mm}$, $W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}$, $W > 0.5\text{mm}$ is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			



12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 $D = (L + W) / 2$ <p>D ≤ 0.3mm, Allowed 0.3mm < D ≤ 0.5mm, N ≤ 5 D > 0.5mm, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 <p>X ≤ 3mm, Y ≤ 0.5mm</p>  <p>2mm ≤ X or 2mm ≤ Y not Allow</p>  <p>W ≤ 0.1mm, L ≤ 5mm, n ≤ 2 Edge crown: X ≤ 0.3mm, Y ≤ 3mm</p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  <p>Not Allow</p>	MA	Visual / Microscope	Zone B



8	B/W Line	 <p> $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}, W > 0.5\text{mm}$ is not allowed </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: $X \leq 3\text{mm}, Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	$D \leq 0.25\text{mm}$, allow $0.25\text{mm} < D \leq 0.4\text{mm}, n \leq 4$ allow $D > 0.4\text{mm}$ is not allowed ($n \leq 8$ items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives $H \leq$ PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 0.5\text{mm}$. $n \leq 5$	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	
14	Silicon glue	Thickness \leq PS surface(With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.	MI	Visual Inspection	Zone B
15	Warp degree (TFT substrate)	 <p> $t \leq 1.5\text{mm}$ </p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	



13. Packaging

<h2 style="margin: 0;">EPD PACKING INSTRUCTION</h2> <p style="margin: 0;">OKRA-QS. D-010</p>						DATE	
						DESIGN	
						CHECKED	
						APPROVED	

P/N	Customer Code	Ref. P/N	Type	PKG Method	Marking	Surface Marks	Pull Tape
OKRA420			GLASS	Blister	BACK	None	YES

Packing Materials List					9PCS/LAYER, 20LAYER/CTN, TOTAL 180PCS/CTN.
List	Model	Materials	Q'ty	Unit	Pull tape:
Carton	7# 417*362*229 mm	corrugate	1	Piece	
Inner Carton	7#(INNER)400*343 *95 mm	corrugate	2	Piece	
Blister	OKRA0420A02 PET 1.0	PET	22	Piece	
Thin foam	295.6*269.6*T1.8~2.0mm	EPE	20	Piece	
Antistatic vacuum bag	450*590*0.075		2	Piece	
Foam board	OKRA2251-10	EPE	5	Piece	
PULL TAPE	16*5*T0.05		180	Piece	

Detail:

Blister box:

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22

QUANTITY: 9PCS

The blister box does not need to be rotated

Shipping marks according to customer's requirements

Epaper Identification	
QC:	PASS
Model No.	_____
Quantity.	_____ pcs
Date:	_____
Carton No.	_____ of _____



14. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Product Environmental certification	
ROHS	
REMARK	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
Transport environment	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	