



Specification for 5.83 inch EPD

Model NO. : OKRA0583RWF686F0

OKRA's Confirmation:

| Prepared by | Checked by | Approved by |
|-------------|------------|-------------|
| | | |

Customer approval:

| Customer | Approved by | Date |
|----------|-------------|------|
| | | |



Revision History

| Version | Content | Date | Producer |
|----------------|----------------|-------------|-----------------|
| 2.0 | New release | 2020/11/13 | |
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1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 5.83inch active area contains 648×480 pixels, and has 1-bit white/black 1-bit red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- ◆ 648×480 pixels display
- ◆ High contrast
- ◆ High reflectance
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape, portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor



3. Mechanical Specification

| Parameter | Specifications | Unit | Remark |
|---------------------|----------------------------|-------|---------|
| Screen Size | 5.83 | Inch | |
| Display Resolution | 648(H)×480(V) | Pixel | DPI:138 |
| Active Area | 118.7784×88.22 | mm | |
| Pixel Pitch | 0.1833×0.1838 | mm | |
| Pixel Configuration | Rectangle | | |
| Outline Dimension | 125.4(H)×99.5 (V) ×1.20(D) | mm | |
| Weight | 28.6±0.5 | g | |

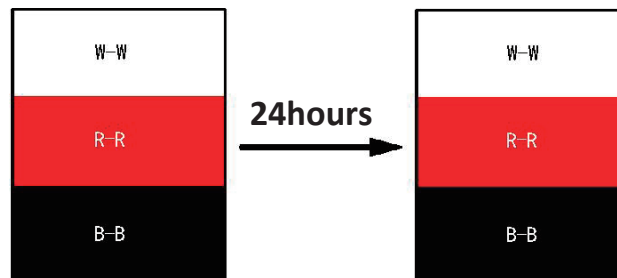
| Symbol | Parameter | Conditions | Min | Typ. | Max | Units | Notes |
|----------|-----------------------------|--|------|--------|-----|-------|------------|
| KS | Black State L* value | | - | 13 | 15 | | 3-1 |
| | Black State A* value | | - | 4 | 6 | | 3-1 |
| | Black Ghosting ΔE | | - | 2 | - | | 3-1 |
| | After 24hour colour changed | | - | 2 | - | | 3-4 |
| WS | White State L* value | | 62 | 65 | - | | 3-1 |
| | White State A* value | | - | 0 | 1 | | 3-1 |
| | White Ghosting ΔE | | - | 2 | - | | 3-1 |
| | After 24hour colour changed | | - | 2 | - | | 3-4 |
| RS | Red State L* value | | 27 | 28 | 32 | | 3-1 |
| | Red State A* value | | 36 | 40 | 45 | | 3-1 |
| | Red Ghosting ΔE | | - | 3 | - | | 3-1 |
| | After 24hour colour changed | | - | 2 | - | | 3-4 |
| T update | Image update time | at 23 °C | - | 17 | - | sec | |
| R | White Reflectivity | White | 30 | 34 | - | % | 3-1 |
| CR | Contrast Ratio | Indoor | 15:1 | 20:1 | - | | 3-1 3-2 |
| GN | 2Grey Level | - | - | - | - | | |
| Life | | Temp:23 ±3°C Humidity:55 ± 10%RH | | 5years | | | 3-3 |

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

3-4. After 24hour Colour Changed:



W: Max $\Delta E(W-W) < 2$, K: Max $\Delta E(B-B) < 2$, R: Max $\Delta E_{ab}(R-R) < 2$.



4.Mechanical Drawing of EPD Module

| | | | | | | |
|---------------|--|------------|------|------------------------------------|--|--|
| Confirmation: | | | | | | |
| | | DATE | REV. | MODIFICATION | | |
| | | 2019-10-12 | A | FIRST ISSUE | | |
| | | 2019-10-23 | B | CHANGE THE FPC GOLDFINGER LOCATION | | |

FRONT VIEW

SIDE VIEW

BACK VIEW

NOTE

- 1 DISPLAY MODULE 5.83" ARRAY FOR EPD
- 2 DRIVER IC: JD79686AB
- 3 RESOLUTION: 648sourceX480gate
- 4 PIXEL SIZE: 0.1833mmX0.1838mm

TOLERANCES UNMARKED

ANGLES ± 5°

.X = ± 0.4mm

.XX = ± 0.20mm

.XXX = ± 0.20mm

TITLE: EPD

PROJECT: OKRA0583RWF686F0

REV: B

DATE: 19.10.23

CUST. P/N:

DWN: XZ FAN

CHK: CC ZHENG

APPR: SY ZHAO

UNIT: mm

3RD ANGLE:

PAGE: 1/1

**5. Input/output Pin Assignment**

| No. | Name | I/O | Description | Remark |
|-----|-------|-----|--|-----------|
| 1 | NC | | Do not connect with other NC pins | Keep Open |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | |
| 3 | RESE | I | Current Sense Input for the Control Loop | |
| 4 | NC | NC | Do not connect with other NC pins | Keep Open |
| 5 | VSH2 | C | Positive Source driving voltage(Red) | |
| 6 | TSCL | O | I2C Interface to digital temperature sensor Clock pin | |
| 7 | TSDA | I/O | I2C Interface to digital temperature sensor Data pin | |
| 8 | BS1 | I | Bus Interface selection pin | Note 5-5 |
| 9 | BUSY | O | Busy state output pin | Note 5-4 |
| 10 | RES# | I | Reset signal input. Active Low. | Note 5-3 |
| 11 | D/C# | I | Data /Command control pin | Note 5-2 |
| 12 | CS# | I | Chip select input pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | |
| 14 | SDA | I/O | Serial Data pin (SPI) | |
| 15 | VDDIO | P | Power Supply for interface logic pins It should be connected with VCI | |
| 16 | VCI | P | Power Supply for the chip | |
| 17 | VSS | P | Ground | |
| 18 | VDD | C | Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS | |
| 19 | VPP | P | FOR TEST | Keep Open |
| 20 | VSH1 | C | Positive Source driving voltage | |
| 21 | VGH | C | Power Supply pin for Positive Gate driving voltage and VSH1 | |
| 22 | VSL | C | Negative Source driving voltage | |
| 23 | VGL | C | Power Supply pin for Negative Gate driving voltage VCOM and VSL | |
| 24 | VCOM | C | VCOM driving voltage | |

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin



Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: Bus interface selection pin

| BS1 State | MCU Interface |
|-----------|--|
| L | 4-lines serial peripheral interface(SPI) - 8 bits SPI |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

6. Electrical Characteristics

6.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|--------------------------|--------|--------------|------|
| Logic supply voltage | VCI | -0.3 to +6.0 | V |
| Logic Input voltage | VIN | -0.3 to TBD | V |
| Operating Temp range | TOPR | 0 to +40 | °C. |
| Storage Temp range | TSTG | -25 to+40 | °C. |
| Optimal Storage Temp | TSTGo | 23±3 | °C. |
| Optimal Storage Humidity | HSTGo | 55±10 | %RH |

Note:

1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. We guarantee the single pixel display quality for 0-35°C, but we only guarantee the barcode readable for 35-40°C.
3. The storage time is within 10 days for -25°C ~ 0°C or 40°C ~ 60°C.
The display screen should be kept white and face up.

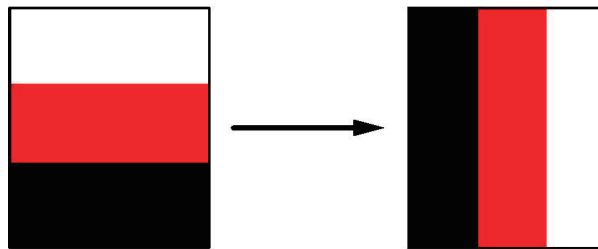


6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|-------------------------------|-----------------------|---|-----------------|----------------------|------|--------------------|------|
| Single ground | V _{SS} | - | | - | 0 | - | V |
| Logic supply voltage | V _{CI} | - | V _{CI} | 2.3 | 3.0 | 3.6 | V |
| Digital/Analog supply voltage | V _{DD} | | V _{DD} | 2.3 | 3.0 | 3.6 | V |
| High level input voltage | V _{IH} | - | - | 0.7 V _{CI} | - | - | V |
| Low level input voltage | V _{IL} | - | - | GND | - | 0.3V _{DD} | V |
| High level output voltage | V _{OH} | I _{OH} = 400uA | - | V _{CI} -0.4 | - | - | V |
| Low level output voltage | V _{OL} | I _{OL} =- 400uA | - | - | - | GND +0.4 | V |
| Typical power | P _{TYP} | V _{CI} =3.0V | - | - | 30 | - | mW |
| Deep sleep mode | P _{STPY} | V _{CI} =3.0V | - | - | | 0.003 | mW |
| Typical operating current | I _{opr_VCI} | V _{CI} =3.0V | - | - | 10 | - | mA |
| Image update time | - | 23 °C | - | - | 17 | - | sec |
| Typical peak current | I _{opr_VCI} | 2.3~3.6V | | | 100 | 200 | mA |
| Sleep mode current | I _{slp_VCI} | DC/DC off No clock No input load Ram data retain | - | - | 20 | - | uA |
| Deep sleep mode current | I _{dslp_VCI} | DC/DC off No clock No input load Ram data not retain | - | - | 1 | 5 | uA |

Notes: 1. The typical power is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OKRA.
4. Electrical measurement: Tektronix oscilloscope - MDO3024,
Tektronix current probe - TCP0030A.



6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name | Data/Command Interface | | Control Signal | | |
|------------------|------------------------|-----|----------------|------|------|
| | SDA | SCL | CS# | D/C# | RES# |
| Bus interface | SDA | SCL | CS# | D/C# | RES# |
| BS1=L 4-wire SPI | SDA | SCL | CS# | D/C# | RES# |
| BS1=H 3-wire SPI | SDA | SCL | CS# | L | RES# |

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

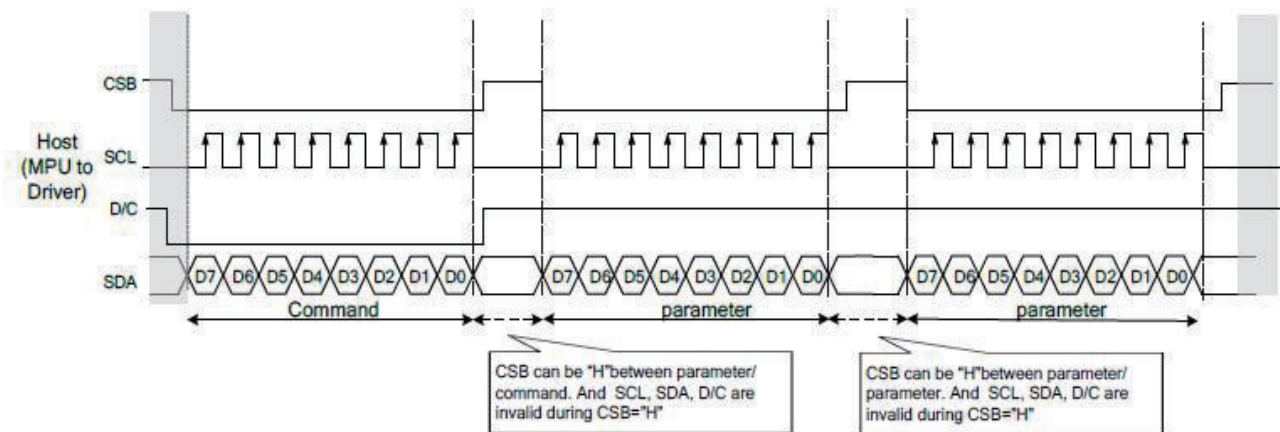
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

| Function | CS# | D/C# | SCL |
|---------------|-----|------|-----|
| Write command | L | L | ↑ |
| Write data | L | H | ↑ |

Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1: 4-wire SPI mode





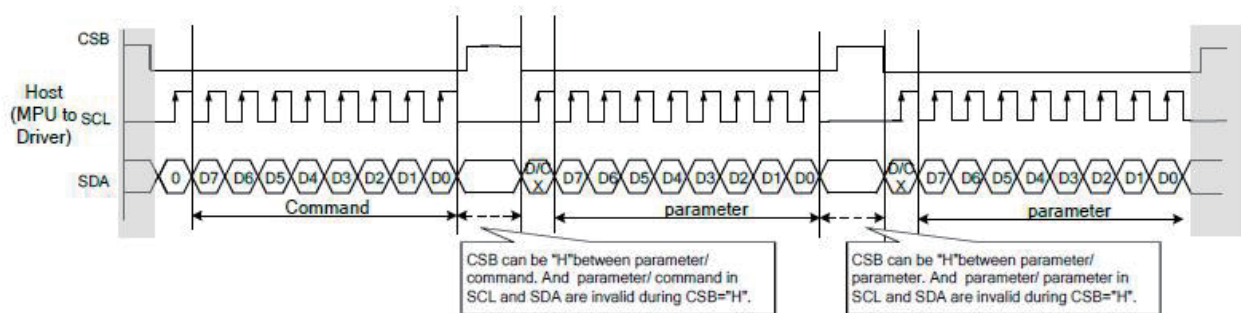
6.3.3 MCU Serial Interface (3-wire SPI)

| Function | CS# | D/C# | SCL |
|---------------|-----|------|-----|
| Write command | L | Tie | ↑ |
| Write data | L | Tie | ↑ |

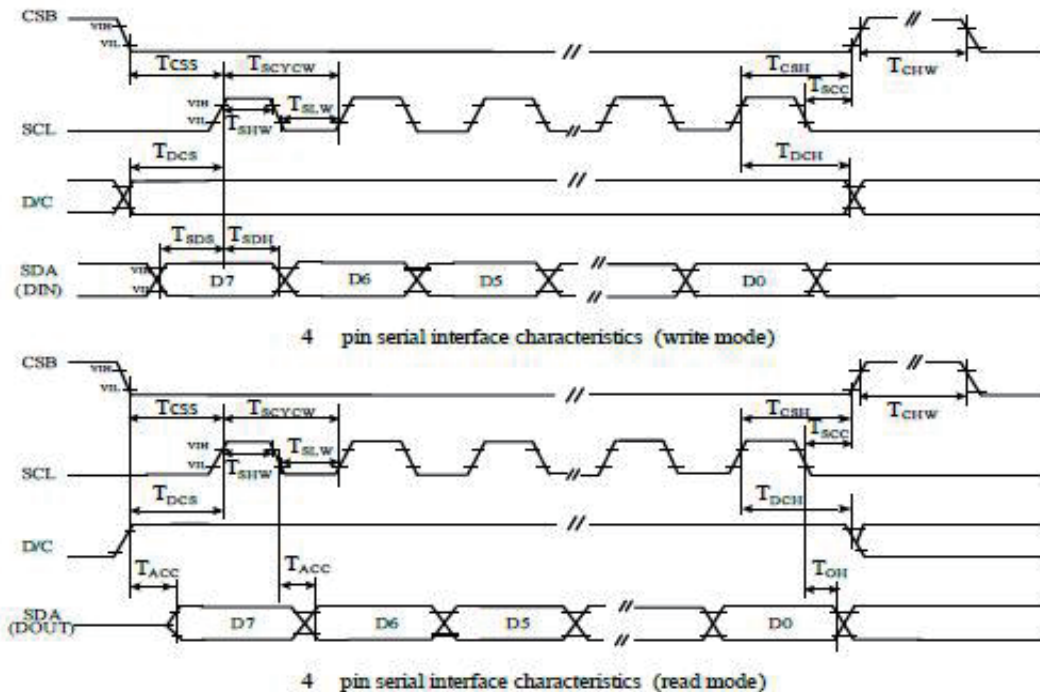
Table 6-3-3: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-2: 3-wire SPI mode



6.3.4 Interface Timing





Serial Interface Timing Characteristics

| Symbol | Signal | Parameter | Min | Typ | Max | Unit |
|--------|---------------------------------|-----------------------------|-----|-----|-----|------|
| Tcss | CS# | Chip Select Setup Time | 100 | - | - | ns |
| Tcsh | | Chip Select Hold Time | 100 | - | - | ns |
| Tscc | | Chip Select Setup Time | 50 | - | - | ns |
| Tchw | | Chip Select Setup Time | 500 | - | - | ns |
| Tscycw | SCLK | Serial clock cycle (write) | 100 | - | - | ns |
| Tshw | | SCL "H" pulse width (write) | 35 | - | - | ns |
| Tslw | | SCL "L" pulse width (write) | 35 | - | - | ns |
| Tscycr | | Serial clock cycle (Read) | 200 | - | - | ns |
| Tshr | | SCL "H" pulse width (Read) | 85 | - | - | ns |
| Tslr | | SCL "L" pulse width (Read) | 85 | - | - | ns |
| Tsds | SDIN (DIN) (DOUT) | Data setup time | 30 | - | - | ns |
| Tsdh | | Data hold time | 30 | - | - | ns |
| Tacc | | Access time | 10 | - | - | ns |
| Toh | | Output disable time | 15 | - | - | ns |



7.Command Table

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|----|---|-----|-----------------|-----------|----------|--------------|--------------|----------|--------------|--------------|--------------|---------|
| 1 | Panel Setting (PSR) | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H |
| | | W | 1 | RES[1] | RES[0] | REG-EN | BWR | UD | SHL | SHD-N | RST-N | 8Fh |
| 2 | Power Setting (PWR) | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H |
| | | W | 1 | - | - | - | - | - | - | VDS_EN | VDG_EN | 03h |
| | | W | 1 | | | - | - | VCOM_HV | VGHL_L V [2] | VGHL_L V [1] | VGHL_L V [0] | 00h |
| | | W | 1 | | | VSH [5] | VSH [4] | VSH [3] | VSH [2] | VSH [1] | VSH [0] | 3Fh |
| | | W | 1 | | | VSL [5] | VSL [4] | VSL [3] | VSL [2] | VSL [1] | VSL [0] | 3bh |
| | | W | 1 | | VSHR [6] | VSHR [5] | VSHR [4] | VSHR [3] | VSHR [2] | VSHR [1] | VSHR [0] | 0Fh |
| | | 3 | Power OFF (POF) | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 4 | Power OFF Sequence Setting(PFS) | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03H |
| | | W | 1 | - | - | T_VDS_OFF[1] | T_VDS_OFF[0] | | | | | 00h |
| 5 | Power ON (PON) | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04H |
| 6 | Power ON Measure Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05H |
| 7 | Booster Soft Start (BTST) | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06H |
| | | W | 1 | BT_PHA_7 | BT_PHA_6 | BT_PHA_5 | BT_PHA_4 | BT_PHA_3 | BT_PHA_2 | BT_PHA_1 | BT_PHA_0 | 17h |
| | | W | 1 | BT_PHB_7 | BT_PHB_6 | BT_PHB_5 | BT_PHB_4 | BT_PHB_3 | BT_PHB_2 | BT_PHB_1 | BT_PHB_0 | 17h |
| | | W | 1 | - | - | BT_PHC_5 | BT_PHC_4 | BT_PHC_3 | BT_PHC_2 | BT_PHC_1 | BT_PHC_0 | 17h |
| 8 | Deep Sleep(DSLP) | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07H |
| | | W | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5h |
| 9 | Data Start Transmission 1 (DTM1) | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00H |
| 10 | Data Stop (DSP) | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11H |
| | | R | 1 | Data_flag | - | - | - | - | - | - | - | -- |
| 11 | Display Refresh (DRF) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |
| 12 | Data Start transmission 2(DTM2) | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |
| 13 | Partial Data Start transmission1 (PDTM1) | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |
| 14 | Partial Data Start transmission 2 (PDTM2) | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |
| 15 | Partial Display Refresh(PDRF) | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |
| 16 | LUT for VCOM (LUT1) | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |
| 17 | White to White LUT (LUTWW) | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |
| 18 | Black to White LUT (LUTBW/LUTR) | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22H |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h |



| | | | | | | | | | | | | | |
|----|-------------------------------------|---|---|--------------|-------------|-------------|-------------|-------------------|-----------|------------------|--------------|-----|-----|
| 19 | White to Black LUT (LUTWB/LUTW) | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23H | |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h | |
| 20 | Black to Black LUT (LUTBB/LUTB) | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24H | |
| | | W | 1 | # | # | # | # | # | # | # | # | 00h | |
| 21 | LUTC option | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25H | |
| | | W | 1 | | | | | | | | XON [9:8] | 00h | |
| | | W | 1 | XON [7:0] | | | | | | | | | 00h |
| | | W | 1 | | | | | | | | ST_CHV [9:8] | 00h | |
| | | W | 1 | ST_CHV [7:0] | | | | | | | | | 00h |
| 22 | Set Vcom/Red states | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26H | |
| | | W | 1 | 0 | 0 | | | vcom_stg_sel[1:0] | | b2w_stg_sel[1:0] | | 00h | |
| 23 | OSC control (OSC) | W | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30H | |
| | | W | 1 | | | M[2:0] | | | N[2:0] | | | 3Ah | |
| 24 | Temperature Sensor Command (TSC) | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40H | |
| | | R | 1 | D10/TS [7] | D9/TS[6] | D8/TS[5] | D7/TS[4] | D6/TS[3] | D5/TS[2] | D4/TS[1] | D3/TS[0] | -- | |
| | | R | 1 | D2 | D1 | D0 | - | - | - | - | - | -- | |
| 25 | Temperature Sensor Calibration(TSE) | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41H | |
| | | W | 1 | TSE | - | - | - | TO[3] | TO[2] | TO[1] | TO0] | 00h | |
| 26 | Temperature Sensor Write (TSW) | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42H | |
| | | W | 1 | WATTR [7] | WATTR [6] | WATTR [5] | WATTR [4] | WATTR [3] | WATTR [2] | WATTR [1] | WATTR [0] | 00h | |
| | | W | 1 | WMSB [7] | WMSB [6] | WMSB [5] | WMSB [4] | WMSB [3] | WMSB [2] | WMSB [1] | WMSB [0] | 00h | |
| | | W | 1 | WLSB[7] | WLSB[6] | WLSB[5] | WLSB[4] | WLSB[3] | WLSB[2] | WLSB[1] | WLSB[0] | 00h | |
| 27 | Temperature Sensor Read (TSR) | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43H | |
| | | R | 1 | RMSB[7] | RMSB[6] | RMSB[5] | RMSB[4] | RMSB[3] | RMSB[2] | RMSB[1] | RMSB[0] | - | |
| | | R | 1 | RLSB[7] | RLSB[6] | RLSB[5] | RLSB[4] | RLSB[3] | RLSB[2] | RLSB[1] | RLSB[0] | - | |
| 28 | Vcom and data interval setting(CDI) | W | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50H | |
| | | W | 1 | VBD[1] | VBD[0] | DDX[1] | DDX[0] | CDI[3] | CDI[2] | CDI[1] | CDI[0] | D7h | |
| 29 | Lower Power Detection (LPD) | W | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51H | |
| | | R | 1 | - | - | - | - | - | - | - | LPD | - | |
| 30 | TCON setting (TCON) | W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60H | |
| | | W | 1 | S2G[3] | S2G[2] | S2G[1]- | S2G[0] | G2S[3] | G2S[2] | G2S[1] | G2S[0] | 22h | |
| 31 | TCON resolution (TRES) | W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 61H | |
| | | W | 1 | HRES(7) | HRES(6) | HRES(5) | HRES(4) | HRES(3) | - | - | - | 00h | |
| | | W | 1 | - | - | - | - | - | - | - | VRES(8) | 00h | |
| | | W | 1 | VRES(7) | VRES(6) | VRES(5) | VRES(4) | VRES(3) | VRES(2) | VRES(1) | VRES(0) | 00h | |
| 32 | Source & gate start setting | W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 62H | |
| | | W | 1 | S_start (7) | S_start (6) | S_start (5) | S_start (4) | S_start (3) | - | - | - | 00h | |



| | | | | | | | | | | | | |
|----|-----------------------------|---|---|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|
| | | W | 1 | | | | gscan | | | | G_start [8] | 00h |
| | | W | 1 | G_start (7) | G_start (6) | G_start (6) | G_start (4) | G_start (3) | G_start (2) | G_start (1) | G_start (0) | 00h |
| 33 | Revision (REV) | W | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70H |
| | | R | 1 | REV[7] | REV[6] | REV[5] | REV[4] | REV[3] | REV[2] | REV[1] | REV[0] | - |
| | | R | 1 | REV[15] | REV[14] | REV[13] | REV[12] | REV[11] | REV[10] | REV[09] | REV[08] | - |
| 34 | Get Status(FLG) | W | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71H |
| | | R | 1 | - | PTL_flag | I2C_ERR | I2C_BUSYN | Data_flag | PON | POF | BUSY_N | - |
| 35 | Auto Measurement Vcom (AMV) | W | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 H |
| | | W | 1 | - | - | AMVT [1] | AMVT [0] | XON | AMVS | AMV | AMVE | 10h |
| 36 | Read Vcom Value(VV) | W | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81H |
| | | R | 1 | - | - | VV[5] | VV[4] | VV[3] | VV[2] | VV[1] | VV[0] | - |
| 37 | VCM_DC Setting (VDCS) | W | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82H |
| | | W | 1 | - | - | VCDS[5] | VCDS [4] | VCDS [3] | VCDS [2] | VCDS [1] | VCDS [0] | 1Fh |
| 38 | Program Mode (PGM) | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0H |
| | | W | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5h |
| 39 | Active program(APG) | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1H |
| 40 | Read OTP Data (ROTP) | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A2H |
| | | R | 1 | # | # | # | # | # | # | # | # | - |
| 41 | Force Temperature | W | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5H |
| | | W | 1 | TS_SET [7] | TS_SET [6] | TS_SET [5] | TS_SET [4] | TS_SET [3] | TS_SET [2] | TS_SET [1] | TS_SET [0] | 00h |
| 42 | LVD voltage Select | W | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | E6H |
| | | W | 1 | - | - | - | - | - | - | LVD_SE L[1] | LVD_SE L[0] | 11h |
| 43 | Panel Break Check | W | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | E7H |
| | | R | 1 | - | - | - | - | - | - | - | PSTA | - |
| 44 | Power saving | W | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | E8H |
| | | W | 1 | VCOM_ W[3] | VCOM_ W[2] | VCOM_ W[1] | VCOM_ W[0] | SD_W[3] | SD_W[2] | SD_W[1] | SD_W[0] | 00h |
| 45 | AUTO sequence | W | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | E9H |
| | | W | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 00h |
| 46 | OTP LUT backup1 program | W | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | EBH |
| 47 | Read OTP LUT backup1 | W | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | ECH |
| | | R | 1 | # | # | # | # | # | # | # | # | -- |
| 48 | OTP LUT backup2 program | W | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | EDH |



| | | | | | | | | | | | | |
|----|-------------------------|---|---|---|---|---|---------------|--------------------|--------------------|--------------------|--------------------|-----|
| | | R | 1 | # | # | # | # | # | # | # | # | -- |
| 49 | Read OTP LUT backup2 | W | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | EEH |
| 50 | Checksum Program to OTP | W | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | EFH |
| 51 | Remap LUT | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0H |
| | | W | 1 | - | - | - | bkup_lut_2_en | rmp2_tab_le_sel[3] | rmp2_tab_le_sel[2] | rmp2_tab_le_sel[1] | rmp2_tab_le_sel[0] | 1Fh |
| | | W | 1 | - | - | - | bkup_lut_1_en | rmp1_tab_le_sel[3] | rmp1_tab_le_sel[2] | rmp1_tab_le_sel[1] | rmp1_tab_le_sel[0] | 1Fh |
| 52 | Set OTP program | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1H |
| | | W | 1 | - | - | - | - | - | - | LUT_bank | reg_bank | 03h |
| 53 | Read checksum | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | F2H |
| | | R | 1 | # | # | # | # | # | # | # | # | 00h |
| 54 | Calculate Checksum | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | F3H |

**COMMAND DESCRIPTION**

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: -: Don't Care

1) Panel Setting (PSR) (R00H)

| R00H | Bit | | | | | | | | | |
|---------------|-----|------|--------|--------|--------|-----|----|-----|-------|-------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PSR | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | RES[1] | RES[0] | REG_EN | BWR | UD | SHL | SHD_N | RST_N |

The command defines as :

| Bit | Name | Description |
|-----|----------|--|
| 0 | RST_N | RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating |
| 1 | SHD_N | SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default) |
| 2 | SHL | SHL function 0: Shift left; First data=Sn → Sn-1 → ...→ S2 → Last data=S1. 1: Shift right: First data=S1→ S2 → ...→ Sn-1 → Last data=Sn. (default) |
| 3 | UD | UD function 0: Scan down; First line=Gn→Gn-1 →...→ G2 → Last line=G1. 1: Scan up; First line=G1 →G2 →...→Gn-1 →Last line=Gn. (default) |
| 4 | BWR | Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with BW. Run LU1 only |
| 5 | REG_EN | LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register |
| 7-6 | RES[1,0] | Resolution setting 00: Display resolution is 600x448 01: Display resolution is 640x480 10: Display resolution is 720x540 11: Display resolution is 800x600 (default) |

Notes:

1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.
2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.



2) Power setting Register (PWR) (R01H)

| R01H | Bit | | | | | | | | | |
|---------------|-----|------|----|----------|----------|----------|----------|-------------|-------------|-------------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PWR | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1st Parameter | W | 1 | - | - | - | - | - | - | VDS_EN | VDG_EN |
| 2nd Parameter | W | 1 | - | - | - | - | VCOM_HV | VGHL_LV [2] | VGHL_LV [1] | VGHL_LV [0] |
| 3rd Parameter | W | 1 | - | - | VSH [5] | VSH [4] | VSH [3] | VSH [2] | VSH [1] | VSH [0] |
| 4th Parameter | W | 1 | - | - | VSL [5] | VSL [4] | VSL [3] | VSL [2] | VSL [1] | VSL [0] |
| 5th Parameter | W | 1 | - | VSHR [6] | VSHR [5] | VSHR [4] | VSHR [3] | VSHR [2] | VSHR [1] | VSHR [0] |

The command defines as :

1st Parameter:

| Bit | Name | Description |
|-----|--------|--|
| 0 | VDG_EN | Gate power selection. 0 : External VDMS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default) |
| 1 | VDS_EN | Source power selection. 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL. (default) |

2nd Parameter:

| Bit | Name | Description |
|-----|---------|--|
| 2-0 | VGHL_LV | VGHL_LV Voltage Level. 000: VGH=20 v, VGL=-20v (default) 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v 110: VGH=14 v, VGL=-14v 111: VGH=13 v, VGL=-13v |
| 3 | VCOM_HV | VCOM Voltage Level 0: VCOMH=VSH+VCOMDC, VCOML=VSL+VCOMDC (default) 1: VCOMH=VGH, VCOML=VGL |

3rd Parameter: Internal VSH power selection for B/W LUT. (Default value: 11111b)

| Bit | Name | Description |
|-----|------|---|
| 5-0 | VSH | Internal VSH power selection. 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v 010111: 7.0V 011000: 7.2 V 011001: 7.4 V 111010: 14.0V 111011: 14.2 V 111100: 14.4V 111101: 14.6V 111110: 14.8V 111111: 15.0V |



4th Parameter: Internal VSL power selection for B/W LUT. (Default value: 111111b)

| Bit | Name | Description |
|-----|------|--|
| 5-0 | VSL | Internal VSL power selection. 000000: -2.4 v 000001: -2.6 v 000010: -2.8 v 000011: -3.0 v 010111: -7.0V 011000: -7.2 V 011001: -7.4 V 111010 :-14.0V 111011: -14.2 V 111100: -14.4 V 111101: -14.6V 111110: -14.8V 111111: -15.0V |

5th Parameter: Internal VSHR power selection for Red LUT. (Default value: 00001111b)

| Bit | Name | Description |
|-----|------|---|
| 6-0 | VSHR | Internal VSL power selection. 0000000: 2.4 v 0000001: 2.5 v 0000010: 2.6 v 0000011: 2.7 v 0101110: 7.0 V 0101111: 7.1 V 0110000: 7.2 V 1010001: 10.5V 1010010: 10.6 V 1010011: 10.7 V 1010100: 10.8V 1010101: 10.9V 1010110: 11.0V |

Notes: VSH>VSHR

3) Power OFF Command (POF)(R02H)

| R02H | Bit | | | | | | | | | |
|-----------|-----|------|----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| POF | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

The command defines as :

After power off command, driver will power off base on power off sequence.

After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will rise from low to high.

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will keep floating.

4) Power off Sequence Setting Register (PFS)(R03H)

| R03H | Bit | | | | | | | | | |
|---------------|-----|------|----|----|------------|-------------|------------|------------|-------------|-------------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PFS | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1st Parameter | W | 1 | - | - | Vsh_off[1] | Vsh_off [0] | Vsl_off[1] | vsl_off[0] | vshr_off[1] | vshr_off[0] |

The command defines as :



| Bit | Name | Description |
|-----|----------|--|
| 1-0 | vshr_off | 00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms |
| 3-2 | vsl_off | 00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms |
| 5-4 | vsh_off | 00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms |

5) Power ON Command (PON)(R04H)

| R04H | Bit | | | | | | | | | |
|-----------|-----|------|----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PON | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

The command defines as :

After power on command, driver will power on base on power on sequence.

After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.

6) Power ON Measure Command(PMES)(R05H)

| R05H | Bit | | | | | | | | | |
|-----------|-----|------|----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PMES | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

The command defines as :

If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).

7) Booster Soft Start Command(BTST)(R06H)

| R01H | Bit | | | | | | | | | |
|---------------------------|-----|------|---------|---------|---------|---------|---------|---------|---------|---------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PWR | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 st Parameter | W | 1 | BT_PHA7 | BT_PHA6 | BT_PHA5 | BT_PHA4 | BT_PHA3 | BT_PHA2 | BT_PHA1 | BT_PHA0 |
| 2 nd Parameter | W | 1 | BT_PHB7 | BT_PHB6 | BT_PHB5 | BT_PHB4 | BT_PHB3 | BT_PHB2 | BT_PHB1 | BT_PHB0 |
| 3 rd Parameter | W | 1 | - | - | BT_PHC5 | BT_PHC4 | BT_PHC3 | BT_PHC2 | BT_PHC1 | BT_PHC0 |

The command define as follows:

1st Parameter:

| Bit | Name | Description |
|-----|------------------------------|--|
| 2-0 | Driving strength of phase A | 000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8 |
| 5-3 | | 000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8 |
| 7-6 | Soft start period of phase A | 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS |



2nd Parameter:

| Bit | Name | Description |
|-----|------------------------------|--|
| 2-0 | Driving strength of phase B | 000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8 |
| 5-3 | | 000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8 |
| 7-6 | Soft start period of phase B | 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS |

3rd Parameter:

| Bit | Name | Description |
|-----|--|---|
| 2-0 | Minimum OFF time setting of GDR in phase C | 000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8 |
| 5-3 | Driving strength of phase C | 000: Strength 1 001: Strength 2 010: Strength 3 (default) <input type="button" value="截图(Alt + A)"/> 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8 |

8) Deep Sleep (DSLPR)(R07H)

| R07H | Bit | | | | | | | | | |
|---------------|-----|------|----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DSLPR | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1st Parameter | W | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

The command define as follows:

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

9) Data Start transmission 1 Register(DTM1)(R10H)

| R10H | Bit | | | | | | | | | |
|---------------|-----|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DTM1 | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | KPixel1 | KPixel2 | KPixel3 | KPixe4 | KPixel5 | KPixel6 | KPixel7 | KPixel8 |
| 2nd Parameter | W | 1 | | | | | | | | |
| ... | W | 1 | | | | | | | | |
| Mth Parameter | W | 1 | KPixel(n-7) | KPixel(n-6) | KPixel(n-5) | KPixel(n-4) | KPixel(n-3) | KPixel(n-2) | KPixel(n-1) | KPixel(n) |

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

**10) Display Refresh Command(DRF)(R12H)**

| R12H | | | Bit | | | | | | | |
|-----------|-----|------|-----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DRF | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

The command defines as :

While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become “0” .

11) Data Start transmission 2 Register (DTM2)(R13H)

| R13H | | | Bit | | | | | | | |
|---------------|-----|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DTM2 | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1st Parameter | W | 1 | KPixel1 | KPixel2 | KPixel3 | KPixel4 | KPixel5 | KPixel6 | KPixel7 | KPixel8 |
| 2nd Parameter | W | 1 | | | | | | | | |
| ... | W | 1 | | | | | | | | |
| Mth Parameter | W | 1 | KPixel(n-7) | KPixel(n-6) | KPixel(n-5) | KPixel(n-4) | KPixel(n-3) | KPixel(n-2) | KPixel(n-1) | KPixel(n) |

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

12) LUT for VCOM (LUTC)(R20H)

| R20H | | | Bit | | | | | | | |
|---------------------|-----|------|---------------------------|----|---------------------------|----|---------------------------|----|--------------------------|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LUTC | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | 1st Level selection [1:0] | | 2nd Level selection [1:0] | | 3rd Level selection [1:0] | | 4th level selection[1:0] | |
| 2nd Parameter | W | 1 | 1st Frame number [7:0] | | | | | | | |
| 3rd Parameter | W | 1 | 2nd Frame number [7:0] | | | | | | | |
| 4thParameter | W | 1 | 3rd Frame number[7:0] | | | | | | | |
| 5thParameter | W | 1 | 4th Frame number[7:0] | | | | | | | |
| 6thParameter | W | 1 | Repeat numbers[7:0] | | | | | | | |
| 7th~13th Parameter | W | 1 | 2nd state | | | | | | | |
| ... | W | 1 | 3rd ~9th state | | | | | | | |
| 55th ~60h Parameter | W | 1 | 10th state | | | | | | | |

The command defines as:

This register is set for VCOM LUT.

This command stores VCOM Look-Up Table with 10 states of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG)

If BWR=1 (BW mode), only 7 groups are used.



| define | description |
|-----------------------|--|
| Level selection [1:0] | 00: -VCM_DC 01: VSH+VCM_DC. 10: VSL+VCM_DC. 11: Floating. |
| Frame number [7:0] | 00000000 : 0 frame 00000001: 1 frame ... 11111110: 254 frame 11111111: 255 frame |
| Repeat numbers [7:0] | 00000000 : 0 00000001: 1 ... 11111110: 254 11111111: 255 |

13) White to White LUT Register(LUTWW)(R21H)

| R21H | Bit | | | | | | | | | | |
|---------------------|-----|------|---------------------------|----|---------------------------|----|---------------------------|----|--------------------------|----|--|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| LUTWW | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | |
| 1st Parameter | W | 1 | 1st Level selection [1:0] | | 2nd Level selection [1:0] | | 3rd Level selection [1:0] | | 4th level selection[1:0] | | |
| 2nd Parameter | W | 1 | 1st Frame number [7:0] | | | | | | | | |
| 3rd Parameter | W | 1 | 2nd Frame number [7:0] | | | | | | | | |
| 4thParameter | W | 1 | 3rd Frame number[7:0] | | | | | | | | |
| 5thParameter | W | 1 | 4th Frame number[7:0] | | | | | | | | |
| 6thParameter | W | 1 | Repeat numbers[7:0] | | | | | | | | |
| 7th~13th Parameter | W | 1 | 2nd state | | | | | | | | |
| ... | W | 1 | 3rd ~9th state | | | | | | | | |
| 55th ~60h Parameter | W | 1 | 10th state | | | | | | | | |

The command defines as:

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

| define | description |
|-----------------------|--|
| Level selection [1:0] | 00: GND 01: VSH 10: VSL 11: VSHR |
| Frame number [7:0] | 00000000 : 0 frame 00000001: 1 frame ... 11111110: 254 frame 11111111: 255 frame |
| Repeat numbers [7:0] | 00000000 : 0 time 00000001: 1 time ... 11111110: 254 times 11111111: 255 times |

14) Black to White LUT or Red LUT Register(LUTBW/LUTR) (R22H)

| R22H | Bit | | | | | | | | | | |
|---------------|-----|------|---------------------------|----|---------------------------|----|---------------------------|----|--------------------------|----|--|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| LUTBW/LUTR | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | |
| 1st Parameter | W | 1 | 1st Level selection [1:0] | | 2nd Level selection [1:0] | | 3rd Level selection [1:0] | | 4th level selection[1:0] | | |
| 2nd Parameter | W | 1 | 1st Frame number [7:0] | | | | | | | | |
| 3rd Parameter | W | 1 | 2nd Frame number [7:0] | | | | | | | | |
| 4thParameter | W | 1 | 3rd Frame number[7:0] | | | | | | | | |
| 5thParameter | W | 1 | 4th Frame number[7:0] | | | | | | | | |
| 6thParameter | W | 1 | Repeat numbers[7:0] | | | | | | | | |
| 7th~13th | W | 1 | 2nd state | | | | | | | | |



| | | | |
|---------------------|---|---|----------------|
| Parameter | | | |
| ... | W | 1 | 3rd ~9th state |
| 55th ~60h Parameter | W | 1 | 10th state |

The command defines as:

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

| define | description |
|-----------------------|---|
| Level selection [1:0] | 00: GND 01: VSH 10: VSL 11: VSHR |
| Frame number [7:0] | 00000000 : 0 frame 00000001 : 1 frame 11111110 : 254 frame 11111111 : 255 frame |
| Repeat numbers [7:0] | 00000000 : 0 time 00000001 : 1 time 11111110 : 254 times 11111111 : 255 times |

15) White to Black LUT or White LUT Register(LUTWB/LUTW)(R23H)

| R23H | Bit | | | | | | | | | |
|---------------------|-----|------|---------------------------|----|---------------------------|----|---------------------------|----|--------------------------|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LUTWB/LUTW | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1st Parameter | W | 1 | 1st Level selection [1:0] | | 2nd Level selection [1:0] | | 3rd Level selection [1:0] | | 4th level selection[1:0] | |
| 2nd Parameter | W | 1 | 1st Frame number [7:0] | | | | | | | |
| 3rd Parameter | W | 1 | 2nd Frame number [7:0] | | | | | | | |
| 4thParameter | W | 1 | 3rd Frame number[7:0] | | | | | | | |
| 5thParameter | W | 1 | 4th Frame number[7:0] | | | | | | | |
| 6thParameter | W | 1 | Repeat numbers[7:0] | | | | | | | |
| 7th~13th Parameter | W | 1 | 2nd state | | | | | | | |
| ... | W | 1 | 3rd ~9th state | | | | | | | |
| 55th ~60h Parameter | W | 1 | 10th state | | | | | | | |

The command defines as:

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

| define | description |
|-----------------------|---|
| Level selection [1:0] | 00: GND 01: VSH 10: VSL 11: VSHR |
| Frame number [7:0] | 00000000 : 0 frame 00000001 : 1 frame 11111110 : 254 frame 11111111 : 255 frame |
| Repeat numbers [7:0] | 00000000 : 0 time 00000001 : 1 time 11111110 : 254 times 11111111 : 255 times |

16) Black to Black LUT or Black LUT Register(LUTBB/LUTB)(R24H)

| R24H | Bit | | | | | | | | | |
|---------------|-----|------|---------------------------|----|---------------------------|----|---------------------------|----|--------------------------|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LUTBB/LUTB | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1st Parameter | W | 1 | 1st Level selection [1:0] | | 2nd Level selection [1:0] | | 3rd Level selection [1:0] | | 4th level selection[1:0] | |



| | | | |
|---|---|---|------------------------|
| 2 nd Parameter | W | 1 | 1st Frame number [7:0] |
| 3 rd Parameter | W | 1 | 2nd Frame number [7:0] |
| 4 th Parameter | W | 1 | 3rd Frame number [7:0] |
| 5 th Parameter | W | 1 | 4th Frame number [7:0] |
| 6 th Parameter | W | 1 | Repeat numbers [7:0] |
| 7 th ~13 th Parameter | W | 1 | 2nd state |
| ... | W | 1 | 3rd ~9th state |
| 55 th ~60 ^h Parameter | W | 1 | 10th state |

The command defines as:

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

| define | description |
|-----------------------|---|
| Level selection [1:0] | 00: GND 01: VSH 10: VSL 11: VSHR |
| Frame number [7:0] | 00000000 : 0 frame 00000001 : 1 frame 11111110 : 254 frame 11111111 : 255 frame |
| Repeat numbers [7:0] | 00000000 : 0 time 00000001 : 1 time 11111110 : 254 times 11111111 : 255 times |

17) LUTC option(LUTC Option)(R25H)

| R25H | | | Bit | | | | | | | |
|---------------------------|-----|------|--------------|----|----|----|----|----|--------------|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LUTC option | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 st Parameter | W | 1 | | | | | | | XON [9:8] | |
| 2 nd Parameter | W | 1 | XON [7:0] | | | | | | | |
| 3 rd Parameter | W | 1 | | | | | | | VCOM_H [9:8] | |
| 4 th Parameter | W | 1 | VCOM_H [7:0] | | | | | | | |

The command defines as:

This register is set for VCOM LUT.

| | |
|-------------|---|
| XON[9:0] | All Gate ON 000000000: No all gate on. 000000001: State1 gate power on 111111111: State1~10 all gate power on |
| VCOM_H[9:0] | Control VCOM Power as High 000000000: No VCOM High voltage 000000001: State1 VCOM High voltage 111111111: State1~10 VCOM High voltage |

18) Set VCOM/Red States(SET_STG) (R26H)

| R26H | | | Bit | | | | | | | |
|---------------------------|-----|------|-----|----|----|----|-------------------|----|------------------|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SET_STG | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 st Parameter | W | 1 | | | - | - | vcom_stg_sel[1:0] | | b2w_stg_sel[1:0] | |

This command is used to set VCOM/Red LUT states

Function of vcom_stg_sel [1:0]/ b2w_stg_sel[1:0] are shown below



| Value | Stages |
|-------|--------|
| 00 | 7 |
| 01 | 8 |
| 10 | 9 |
| 11 | 10 |

Default is set as 7 stages.

19) OSC control Register(OSC)(R30H)

| R30H | | | Bit | | | | | | | |
|---------------|-----|------|-----|----|--------|----|----|--------|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OSC | W | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | - | - | M[2:0] | | | N[2:0] | | |

The command defines as:

The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

| M | N | Frame rate | M | N | Frame rate | M | N | Frame rate | M | N | Frame rate |
|---|---|------------|---|---|------------|---|---|------------|---|---|----------------|
| 1 | 1 | 29HZ | 3 | 1 | 86HZ | 5 | 1 | 150HZ | 7 | 1 | 200HZ |
| | 2 | 14HZ | | 2 | 43HZ | | 2 | 72HZ | | 2 | 100HZ |
| | 3 | 10HZ | | 3 | 29HZ | | 3 | 48HZ | | 3 | 67HZ |
| | 4 | 7HZ | | 4 | 21HZ | | 4 | 36HZ | | 4 | 50HZ (default) |
| | 5 | 6HZ | | 5 | 17HZ | | 5 | 29HZ | | 5 | 40HZ |
| | 6 | 5HZ | | 6 | 14HZ | | 6 | 24HZ | | 6 | 33HZ |
| | 7 | 4HZ | | 7 | 12HZ | | 7 | 20HZ | | 7 | 29HZ |
| 2 | 1 | 57HZ | 4 | 1 | 114HZ | 6 | 1 | 171HZ | | | |
| | 2 | 29HZ | | 2 | 57HZ | | 2 | 86HZ | | | |
| | 3 | 19HZ | | 3 | 38HZ | | 3 | 57HZ | | | |
| | 4 | 14HZ | | 4 | 29HZ | | 4 | 43HZ | | | |
| | 5 | 11HZ | | 5 | 23HZ | | 5 | 34HZ | | | |
| | 6 | 10HZ | | 6 | 19HZ | | 6 | 29HZ | | | |
| | 7 | 8HZ | | 7 | 16HZ | | 7 | 24HZ | | | |

20) Temperature Sensor Command(TSC)(R40H)

| R40H | | | Bit | | | | | | | |
|---------------|-----|------|-----------|----------|----------|----------|----------|----------|----------|----------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TSC | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1st Parameter | R | 1 | D10/TS[7] | D9/TS[6] | D8/TS[5] | D7/TS[4] | D6/TS[3] | D5/TS[2] | D4/TS[1] | D3/TS[0] |
| 2nd Parameter | R | 1 | D2 | D1 | D0 | - | - | - | - | - |

The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



| TS[7:0]/D[10:3] | T (°C) | TS[7:0]/D[10:3] | T (°C) | TS[7:0]/D[10:3] | T (°C) |
|-----------------|--------|-----------------|--------|-----------------|--------|
| 11100111 | -25 | 00000000 | 0 | 00011001 | 25 |
| 11101000 | -24 | 00000001 | 1 | 00011010 | 26 |
| 11101001 | -23 | 00000010 | 2 | 00011011 | 27 |
| 11101010 | -22 | 00000011 | 3 | 00011100 | 28 |
| 11101011 | -21 | 00000100 | 4 | 00011101 | 29 |
| 11101100 | -20 | 00000101 | 5 | 00011110 | 30 |
| 11101101 | -19 | 00000110 | 6 | 00011111 | 31 |
| 11101110 | -18 | 00000111 | 7 | 00100000 | 32 |
| 11101111 | -17 | 00001000 | 8 | 00100001 | 33 |
| 11110000 | -16 | 00001001 | 9 | 00100010 | 34 |
| 11110001 | -15 | 00001010 | 10 | 00100011 | 35 |
| 11110010 | -14 | 00001011 | 11 | 00100100 | 36 |
| 11110011 | -13 | 00001100 | 12 | 00100101 | 37 |
| 11110100 | -12 | 00001101 | 13 | 00100110 | 38 |
| 11110101 | -11 | 00001110 | 14 | 00100111 | 39 |
| 11110110 | -10 | 00001111 | 15 | 00101000 | 40 |
| 11110111 | -9 | 00010000 | 16 | 00101001 | 41 |
| 11111000 | -8 | 00010001 | 17 | 00101010 | 42 |
| 11111001 | -7 | 00010010 | 18 | 00101011 | 43 |
| 11111010 | -6 | 00010011 | 19 | 00101100 | 44 |
| 11111011 | -5 | 00010100 | 20 | 00101101 | 45 |
| 11111100 | -4 | 00010101 | 21 | 00101110 | 46 |
| 11111101 | -3 | 00010110 | 22 | 00101111 | 47 |
| 11111110 | -2 | 00010111 | 23 | 00110000 | 48 |
| 11111111 | -1 | 00011000 | 24 | 00110001 | 49 |

This command only actives after R04H(PON) or R05H(PMES)

21) VCOM and DATA interval setting Register(CDI)(R50H)

| R50H | | | Bit | | | | | | | |
|---------------|-----|------|--------|--------|--------|--------|--------|--------|--------|--------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CDI | W | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | VBD[1] | VBD[0] | DDX[1] | DDX[0] | CDI[3] | CDI[2] | CDI[1] | CDI[0] |

The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

| Bit | |
|-----|---|
| 3-0 | Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync |



VBD[1:0] Border data selection.

B/W/Red mode(BWR=0)

| Bit 5-4 | Bit7-6 | Description |
|-------------|--------------|-------------|
| DDX[0] | VBD[1:0] | LUT |
| 0 | 00 | Floating |
| | 01 | LUTR |
| | 10 | LUTW |
| | 11 | LUTB |
| 1 (default) | 00 | LUTB |
| | 01 | LUTW |
| | 10 | LUTR |
| | 11 (default) | Floating |

B/W mode (BWR=1)

| Bit 5-4 | Bit7-6 | description |
|-------------|----------|--------------|
| DDX[0] | VBD[1:0] | LUT |
| 0 | 00 | Floating |
| | 01 | LUTBW (1->0) |
| | 10 | LUTWB (0->1) |
| | 11 | Floating |
| 1 (default) | 00 | Floating |
| | 01 | LUTWB (1->0) |
| | 10 | LUTBW (0->1) |
| | 11 | Floating |

DDX[1:0]: Data polarity

- DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
- DDX[0] for B/W mode

B/W/Red mode(BWR=0)

| Bit 5-4 | Description | |
|--------------|----------------|------|
| DDX[1:0] | Data (Red/B/W) | LUT |
| 00 | 00 | LUTW |
| | 01 | LUTB |
| | 10 | LUTR |
| | 11 | LUTR |
| 01 (default) | 00 | LUTB |
| | 01 | LUTW |
| | 10 | LUTR |
| | 11 | LUTR |
| 10 | 00 | LUTR |
| | 01 | LUTR |
| | 10 | LUTW |
| | 11 | LUTB |
| 11 | 00 | LUTR |
| | 01 | LUTR |
| | 10 | LUTB |
| | 11 | LUTW |

B/W mode (BWR=1)

| Bit 5-4 | Description | |
|-------------|-------------|--------------|
| DDX[0] | Data (B/W) | LUT |
| 0 | 00 | LUTWW (0->0) |
| | 01 | LUTBW(1->0) |
| | 10 | LUTWB(0->1) |
| | 11 | LUTBB(1->1) |
| 1 (default) | 00 | LUTBB(0->0) |
| | 01 | LUTWB(1->0) |
| | 10 | LUTBW(0->1) |
| | 11 | LUTWW(1->1) |

22) TCON setting(TCON)(R60H)

| R60H | Bit | | | | | | | | | |
|---------------|-----|------|----|----|----|----|----|----|----|-----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TCON | W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | - | - | - | - | - | - | - | LPD |

The command define Non-overlap period of gate and source as below:

1st Parameter:



| Bit | Period |
|-------------------|---|
| S2G[3:0]/G2S[3:0] | 0000: 2 clock(default) 0001: 4 clock 0010: 6 clock 0011: 8 clock 0100: 10 clock 0101: 12 clock 0110: 14 clock 0111: 16 clock 1000: 18 clock 1001: 20 clock 1010: 22 clock 1011: 24 clock 1100: 26 clock 1101: 28 clock 1110: 40 clock 1111: 32 clock |

23) Resolution setting(TRES)(R61H)

| R61H | | Bit | | | | | | | | |
|---------------|-----|------|---------|---------|---------|---------|---------|---------|---------|---------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TREAS | W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1st Parameter | W | 1 | | | | | | | HRES(9) | HRES(8) |
| 2nd Parameter | W | 1 | HRES(7) | HRES(6) | HRES(5) | HRES(4) | HRES(3) | - | - | - |
| 3rd Parameter | W | 1 | | | | | | | VRES(9) | VRES(8) |
| 4thParameter | W | 1 | VRES(7) | VRES(6) | VRES(5) | VRES(4) | VRES(3) | VRES(2) | VRES(1) | VRES(0) |

The command define as follows: When using register:

Horizontal display resolution = HRES Vertical display resolution = VRES

Channel disable calculation:

GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1

SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1

EX :128X272

GD: First G active = G0

LAST active GD= 0+272-1= 271; (G271)

SD : First active channel: =S0

LAST active SD=0+16*8-1=127; (S127)

24) Source & gate start setting(TSGS)(R62H)

| R62H | | Bit | | | | | | | | |
|---------------|-----|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| TSGS | W | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1st Parameter | W | 1 | | | | | | | S_Start (9) | S_Start (8) |
| 2nd Parameter | W | 1 | S_Start (7) | S_Start (6) | S_Start (5) | S_Start (4) | S_Start (3) | - | - | - |
| 3rd Parameter | W | 1 | | | | | | | G_Start (9) | G_Start (8) |
| 4thParameter | W | 1 | G_Start (7) | G_Start (6) | G_Start (5) | G_Start (4) | G_Start (3) | G_Start (2) | G_Start (1) | G_Start (0) |

The command define as follows:

1.S_Start [8:0] describe which source output line is the first date line

2.G_Start[8:0] describe which gate line is the first scan line

3.gscan :Gate scan select

0: Normal scan

1: Cascade type 2 scan

Restriction: S_Start should be the multiple of 8



| Bit | Function |
|-----|---|
| 5-0 | Vcom value 000000: -0.1V 000001: -0.15V 000010: -0.2V 111000: -2.9V 111001: -2.95V 111010: -3.0V |

25) Program Mode(PGM)(RA0H)

| RA0H | | | Bit | | | | | | | |
|---------------|-----|------|-----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PTIN | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

The command define as follows:

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

26) Active Program(APG)(RA1H)

| RA1H | | | Bit | | | | | | | |
|-----------|-----|------|-----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| APG | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

The command define as follows:

After this command is transmitted, the programming state machine would be activated.

27) Read OTP Data(ROTP)(RA2H)

| RA2H | | | Bit | | | | | | | |
|------------------------|-----|------|--------------------------------------|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LUTBB/LUTB | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1st Parameter | W | 1 | Dummy | | | | | | | |
| 2nd Parameter | W | 1 | The data of address 0x000 in the OTP | | | | | | | |
| 3rd Parameter | W | 1 | The data of address 0x001 in the OTP | | | | | | | |
| 4thParameter | W | 1 | : | | | | | | | |
| 5thParameter | W | 1 | The data of address (n-1) in the OTP | | | | | | | |
| 6th~ (m-1)th Parameter | W | 1 | ... | | | | | | | |
| mth Parameter | W | 1 | The data of address (n) in the OTP | | | | | | | |

The command define as follows:

The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.

28) Remap LUT command(RM_LUT_CMD)(RF0H)

| RF0H | | | Bit | | | | | | | |
|---------------|-----|------|-----|----|----|-------------|-------------------|-------------------|-------------------|-------------------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RM_LUT_CMD | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1st Parameter | W | 1 | - | - | - | tr10_lut_en | rmp2_table_sel[3] | rmp2_table_sel[2] | rmp2_table_sel[1] | rmp2_table_sel[0] |
| 2nd Parameter | W | 1 | - | - | - | tr9_lut_en | Rmp1_table_sel[3] | Rmp1_table_sel[2] | Rmp1_table_sel[1] | Rmp1_table_sel[0] |

The command is used for indicating backup OTP blocks to remap for LUTs



| Addr (hex) | OTP Bank 0 (3K Bytes) | Addr (hex) | OTP Bank 1 (3K Bytes) |
|------------|--------------------------|------------|--------------------------|
| 00h~0Fh | Temp. segment | C00h~C0Fh | Temp. segment |
| 20h~60h | Default setting | C20h~C60h | Default setting |
| 100h | TR0 WF | D00h | TR0 WF |
| 200h | TR1 WF | E00h | TR1 WF |
| 300h | TR2 WF | F00h | TR2 WF |
| 400h | TR3 WF | 1000h | TR3 WF |
| 500h | TR4 WF | 1100h | TR4 WF |
| 600h | TR5 WF | 1200h | TR5 WF |
| 700h | TR6 WF | 1300h | TR6 WF |
| 800h | TR7 WF | 1400h | TR7 WF |
| 900h | TR8 WF | 1500h | TR8 WF |
| A00h | TR9 WF / Backup 1 | 1600h | TR9 WF / Backup 1 |
| B00h | TR10 WF / Backup 2 | 1700h | TR10 WF / Backup 2 |

1st Parameter:

tr10_lut_en :

| Value | Function |
|-------|--|
| 1 | OTP Address B00h~BFFh is used as "TR10 WF" |
| 0 | OTP Address B00h~BFFh is used as "Backup 2", And you can replace one of TR0 ~TR9. |

rmp2_tab_sel [3:0] :

Only be functional when tr10_lut_en is set "0", target LUTs to be replaced is shown below

| Value | Target LUTs |
|-----------|-------------|
| 0001 | TR0 |
| 0010 | TR1 |
| 0011 | TR2 |
| 0100 | TR3 |
| 0101 | TR4 |
| 0110 | TR5 |
| 0111 | TR6 |
| 1000 | TR7 |
| 1001 | TR8 |
| 1010 | TR9 |
| 1011~1111 | None |

2nd Parameter

tr9_lut_en :

| Value | Function |
|-------|--|
| 1 | OTP Address B00h~BFFh is used as "TR9 WF" |
| 0 | OTP Address B00h~BFFh is used as "Backup 1", And you can replace one of TR0 ~TR8. |

rmp1_tab_sel [3:0]

Only be functional when tr9_lut_en is set "0", target LUTs to be replaced is shown below

| Value | Target LUTs |
|-----------|-------------|
| 0001 | TR0 |
| 0010 | TR1 |
| 0011 | TR2 |
| 0100 | TR3 |
| 0101 | TR4 |
| 0110 | TR5 |
| 0111 | TR6 |
| 1000 | TR7 |
| 1001 | TR8 |
| 1010~1111 | None |

Notice :

If rmp1_tab_sel = rmp2_tab_sel , the control hardware will reload "backup 1" block to replace target LUT.



29) Set OTP program bank(SET_OTP_BANK)(RF1H)

| REEH | Bit | | | | | | | | | |
|---------------|-----|------|----|----|----|----|----|----|-----------|-----------|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SET_OTP_BANK | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1st Parameter | W | 1 | | | - | - | - | - | LUT_bank0 | reg_bank0 |

This command is used to set program bank for registers and LUTs

| Addr (hex) | OTP Bank 0 (3K Bytes) | Addr (hex) | OTP Bank 1 (3K Bytes) |
|------------|-----------------------|------------|-----------------------|
| 00h~0Fh | Temp. segment | C00h~C0Fh | Temp. segment |
| 20h~60h | Default setting | C20h~C60h | Default setting |
| 100h~BFFh | LUTs | D00h~17FFh | LUTs |

reg_bank :

| Value | Function |
|-------|---|
| 1 | Program "Temp. segment" and "Default Setting" in bank 0 |
| 0 | Program "Temp. segment" and "Default Setting" in bank 1 |

LUT_bank :

| Value | Function |
|-------|--------------------------|
| 1 | Program "LUTs" in bank 0 |
| 0 | Program "LUTs" in bank 1 |

30) Read checksum information(RD_CHKSUM)(RF2H)

| RF2H | Bit | | | | | | | | | |
|--------------------|-----|------|--|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RD_CHKSUM | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1st ~9th Parameter | R | 1 | Checksum from "TR0 WF" to "TR8 WF" | | | | | | | |
| 10th Parameter | R | 1 | Checksum of "TR9 WF / backup 1" | | | | | | | |
| 11th Parameter | R | 1 | Checksum of "TR10 WF / backup 2" | | | | | | | |
| 12th Parameter | R | 1 | Checksum comparison result from "TR0 WF" to "TR7 WF" | | | | | | | |
| 13th Parameter | R | 1 | Checksum comparison result from "TR8" and "TR10 WF / backup 2" | | | | | | | |

This command is to read checksum information from OTP.

1st to 11th Parameter : Checksum from "TR0 WF" to "TR10 WF / backup 2"

12th Parameter

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| fault_TR7 | fault_TR6 | fault_TR5 | fault_TR4 | fault_TR3 | fault_TR2 | fault_TR1 | fault_TR0 |

13th Parameter

| D7 | D6 | D5 | D4 | D3 | D2 | | D1 | | D0 |
|----|----|----|----|----|----------------------------|--|---------------------------|--|-----------|
| - | - | - | - | - | fault_TR10 / fault_backup2 | | fault_TR9 / fault_backup1 | | fault_TR9 |

definition of fault_TRx / fault_backup_x

| Value | Function |
|-------|---------------------------------|
| 0 | Checksum comparison : Equal |
| 1 | Checksum comparison : Not Equal |

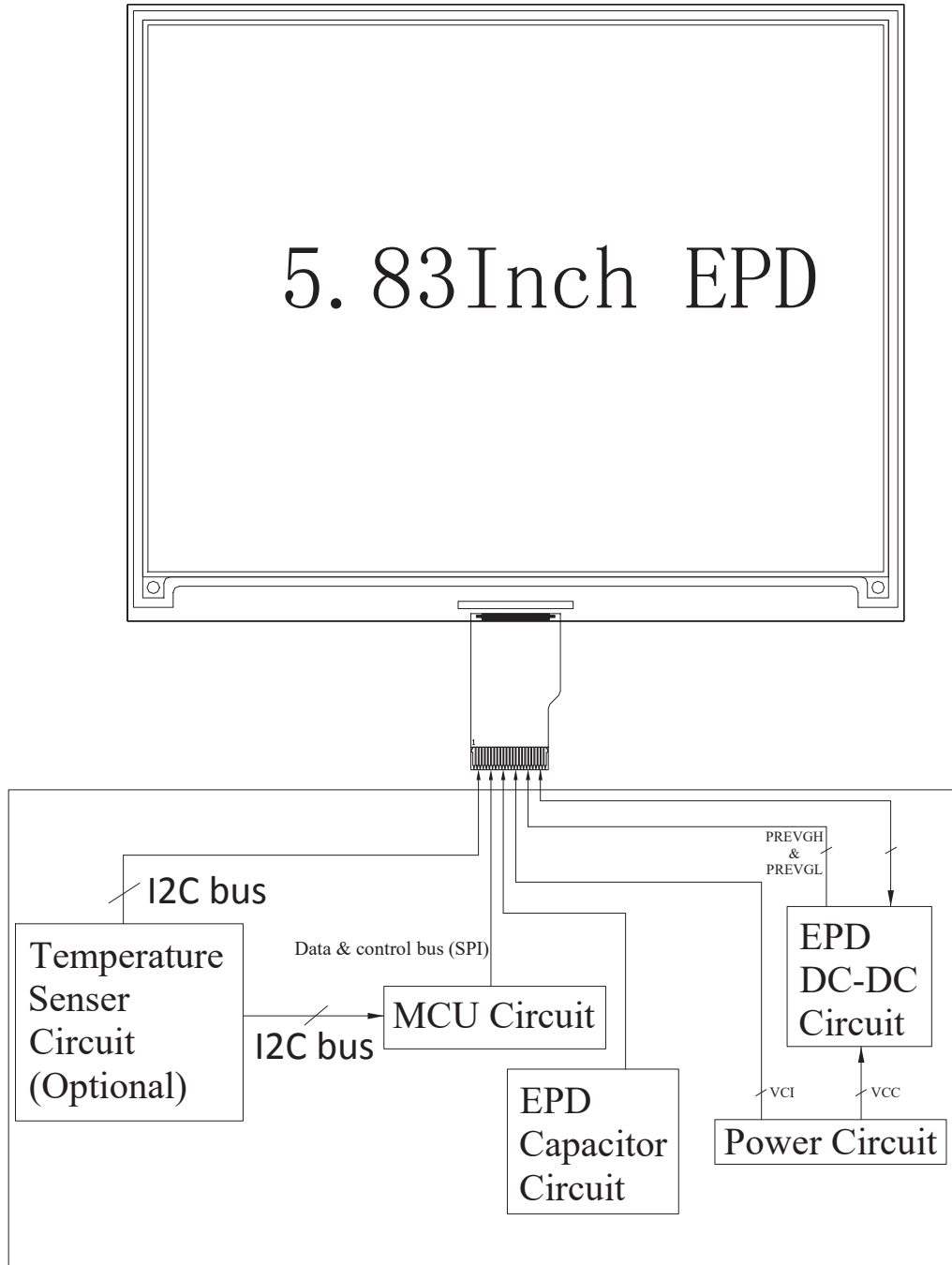
31) RF3H (CAL_CHKSUM): Calculate Checksum

| RF3H | Bit | | | | | | | | | |
|------------|-----|------|----|----|----|----|----|----|----|----|
| Inst/Para | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CAL_CHKSUM | W | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

This command is used to Calculate Checksum of LUT Table

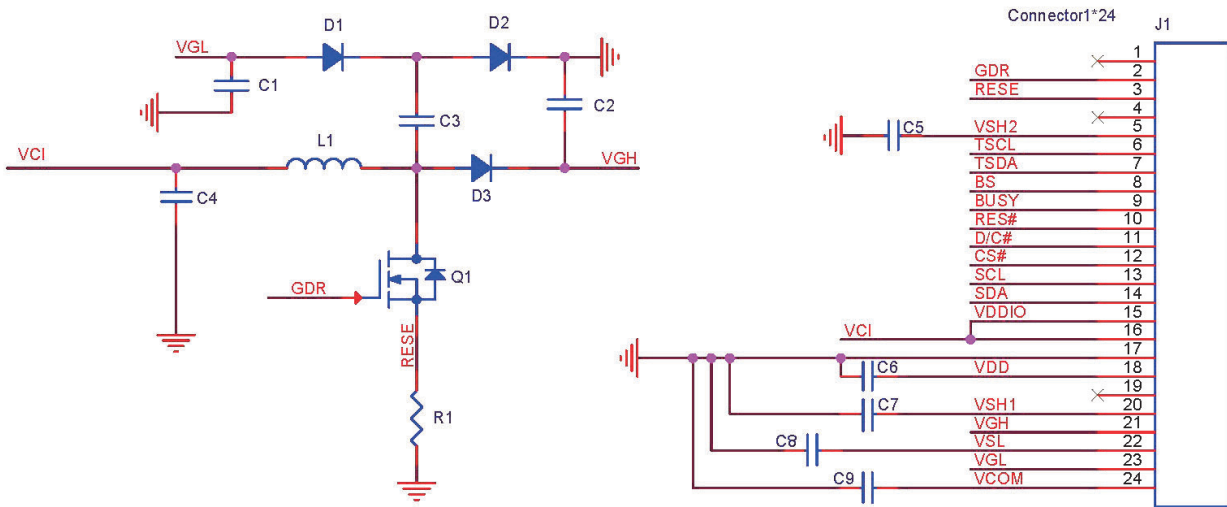


8 Block Diagram





9. Typical Application Circuit with SPI Interface

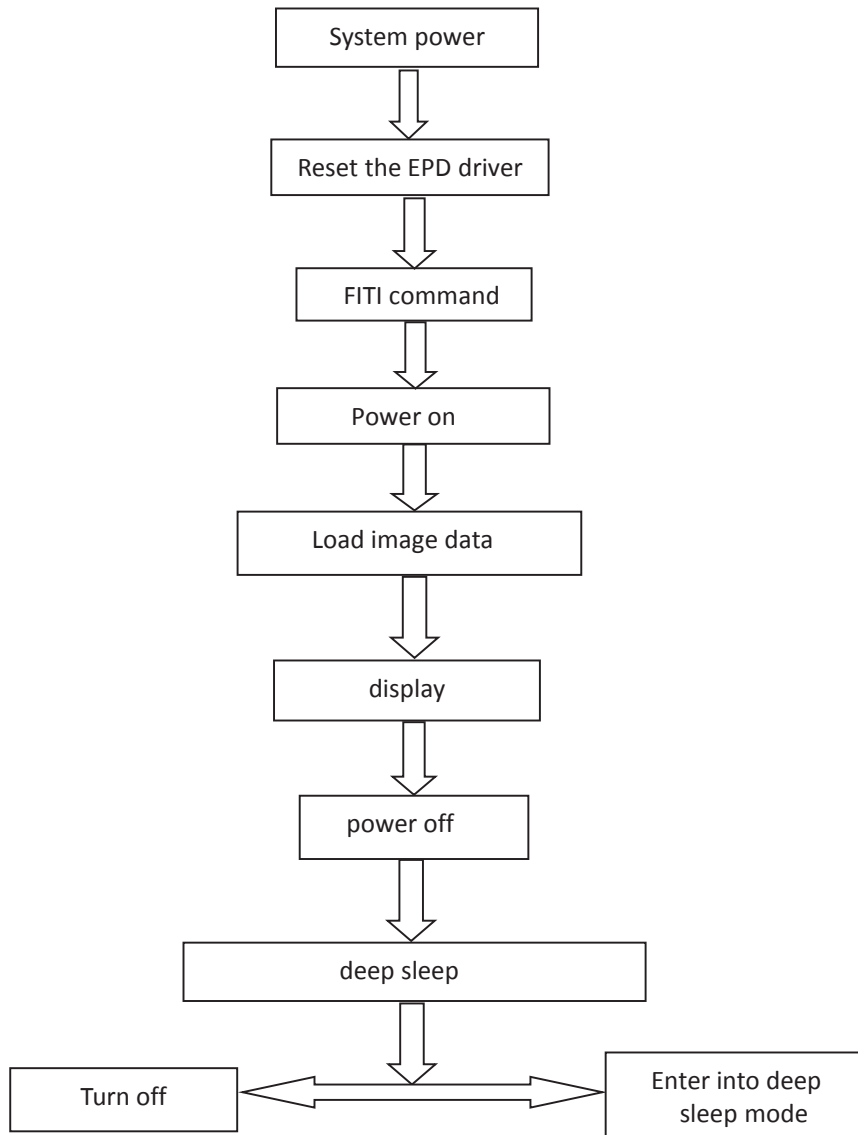


| Part Name | Value | Requirements for spare part |
|----------------|--------|-----------------------------|
| C1 C2 | 4.7uF | 50V |
| C4 C5 C6 C7 C8 | 1uF | 25V |
| C3 C9 | 1uF | 50V |
| R1 | 2.2Ohm | NO |
| D4 D5 D6 | Diode | MBR0503 |
| Q1 | NMOS | Si1304BDL |
| L2 | 47UH | NO |



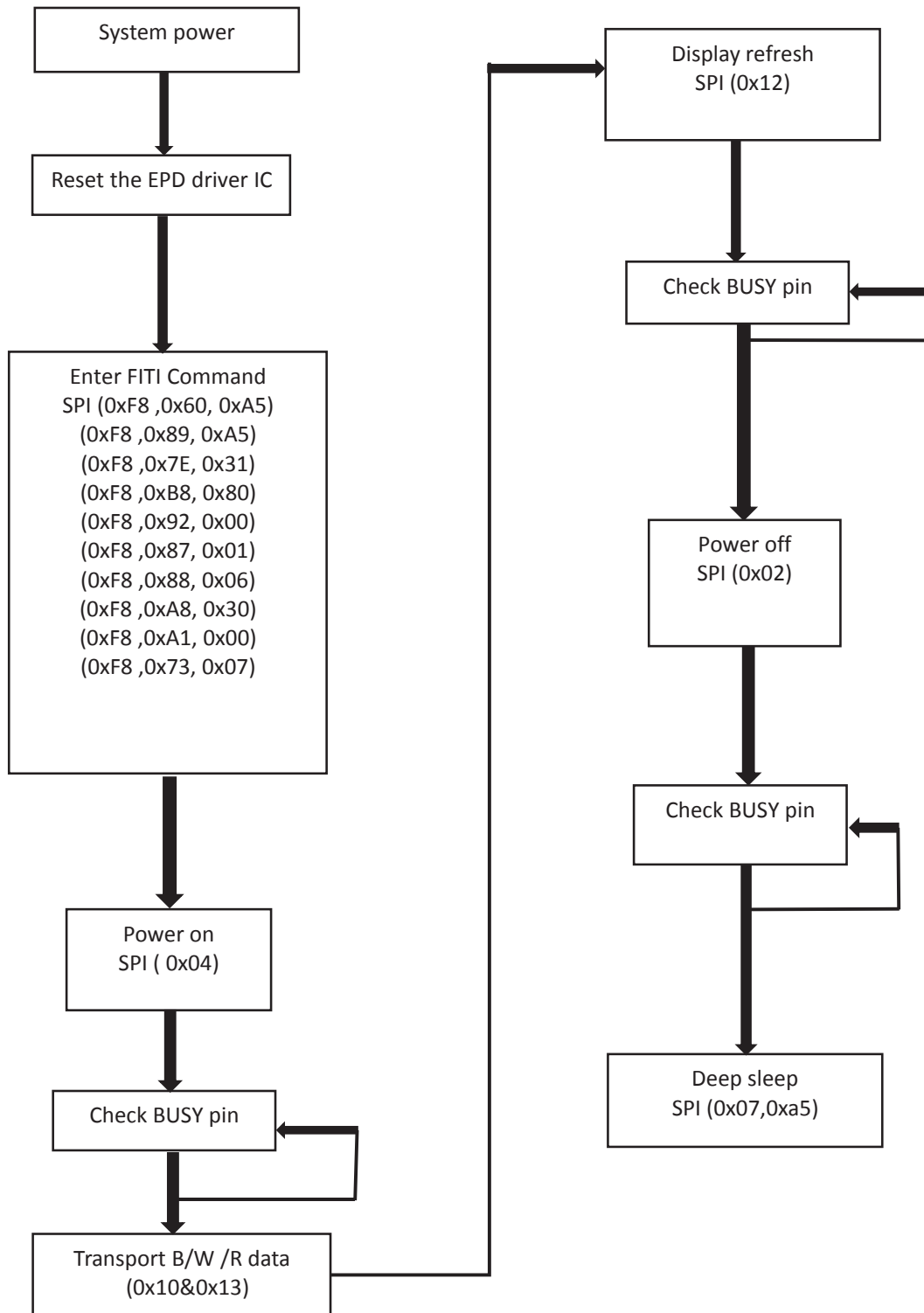
10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow





10.2 LUT from OTP Operation Reference Program Code





11. Reliability Test

| NO | Test items | Test condition |
|----|---|--|
| 1 | Low-Temperature Storage | T = -25°C, 240 h Test in white pattern |
| 2 | High-Temperature Storage | T=60°C, RH=40%, 240h Test in white pattern |
| 3 | High-Temperature Operation | T=40°C, RH=35%, 240h |
| 4 | Low-Temperature Operation | 0°C, 240h |
| 5 | High-Temperature, High-Humidity Operation | T=40°C, RH=80%, 240h |
| 6 | High Temperature, High Humidity Storage | T=50°C, RH=80%, 240h Test in white pattern |
| 7 | Temperature Cycle | 1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern |
| 8 | ESD Gun | Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area) |

Note: 1. Stay white pattern for storage and non-operation test.

2. Operation is black→white-red pattern, the interval is 150s.

3. Put in 20°C--25°C for 1hour after test finished, The function ,appearance and display performance is OK.



12. Quality Assurance

12.1 Environment

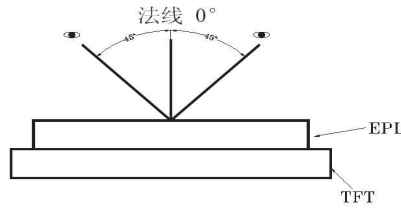
Temperature: 23±3°C

Humidity: 55±10%RH

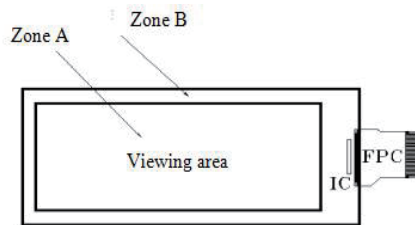
12.2 Illuminance

Brightness: 1200~1500LUX; distance: 20-30CM; Angle: Relate 45° surround.

12.3 Inspect method

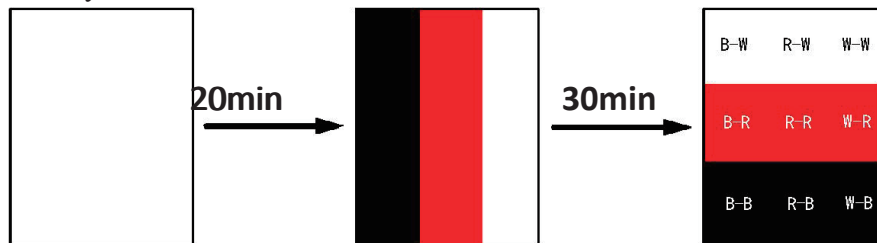


12.4 Display area



12.5 Ghosting test method

Three-color ghosting is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by OKRA.



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

W ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(W-W, R-W), \Delta E_{ab}(W-W, B-W), \Delta E_{ab}(B-W, R-W))$

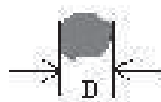
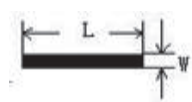
K ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(B-B, W-B), \Delta E_{ab}(B-B, R-B), \Delta E_{ab}(R-B, W-B))$

R ghosting: $\Delta E = \text{Max} (\Delta E_{ab}(R-R, W-R), \Delta E_{ab}(R-R, B-R), \Delta E_{ab}(B-R, W-R))$



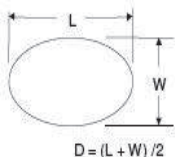
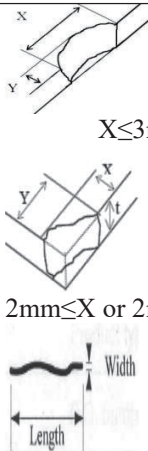
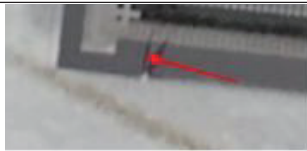
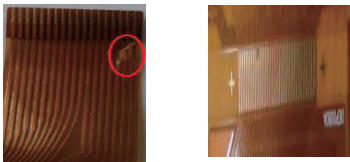
12.6 Inspection standard

12.6.1 Electric inspection standard

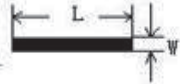
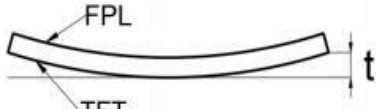
| NO. | Item | Standard | Defect level | Method | Scope |
|-----|--|---|--------------|-------------------------|------------------|
| 1 | Display | Clear display Display complete Display uniform | MA | | |
| 2 | Black/White spots |  $D \leq 0.3\text{mm}$, negligible $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$, Allowed $0.5\text{mm} < D$ Not Allow | | Visual inspection | |
| 3 | Black/White lines (No switch) |  $L \leq 1.0\text{mm}$, $W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}$, $W > 0.5\text{mm}$ is not allowed | MI | Visual/ Inspection card | Zone A |
| 4 | Ghost image | Allowed in switching process | MI | Visual inspection | |
| 5 | Flash dot / Multilateral | Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time | MI | Visual/ Inspection card | Zone A Zone B |
| 6 | Segmented display | Selection segments are all displayed, and other segments are not displayed after the selection segment. | | | |
| 7 | Short circuit/ Circuit break/ Abnormal Display | Not Allow | MA | Visual inspection | Zone A |



12.6.2 Appearance inspection standard

| NO. | Item | Standard | Defect level | Method | Scope |
|-----|---|---|--------------|------------------------|--------------------|
| 1 | B/W spots /Bubble/ Foreign bodies/ Dents |  <p>$D = (L + W) / 2$</p> <p>$D \leq 0.3\text{mm}$, Allowed $0.3\text{mm} < D \leq 0.5\text{mm}$, $N \leq 5$ $D > 0.5\text{mm}$, Not Allow</p> | MI | Visual inspection | Zone A |
| 2 | Glass crack | Not Allow | MA | Visual / Microscope | Zone A Zone B |
| 3 | \Dirty | Allowed if can be removed | MI | | Zone A Zone B |
| 4 | Chips/Scratch/ Edge crown |  <p>$X \leq 3\text{mm}, Y \leq 0.5\text{mm}$</p> <p>$2\text{mm} \leq X$ or $2\text{mm} \leq Y$ not Allow</p> <p>$W \leq 0.1\text{mm}, L \leq 5\text{mm}, n \leq 2$ Edge crown: $X \leq 0.3\text{mm}, Y \leq 3\text{mm}$</p> | MI | Visual / Microscope | Zone A Zone B |
| 5 | TFT Cracks |  <p>Not Allow</p> | MA | Visual / Microscope | Zone A Zone B |
| 6 | Dirty/ foreign body | Allowed if can be removed/ allow | MI | Visual / Microscope | Zone A / Zone B |
| 7 | FPC broken/ FPC oxidation / scratch |  <p>Not Allow</p> | MA | Visual / Microscope | Zone B |



| | | | | | |
|----|--|---|----|---------------------|------------------|
| 8 | B/W Line |  <p> $L \leq 1.0\text{mm}, W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}, W > 0.5\text{mm}$ is not allowed </p> | MI | Visual / Ruler | Zone B |
| 9 | TFT edge bulge /TFT chromatic aberration | <p>TFT edge bulge: $X \leq 3\text{mm}, Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed</p> | MI | Visual / Microscope | Zone A Zone B |
| 10 | Electrostatic point | <p> $D \leq 0.25\text{mm}$, allow $0.25\text{mm} < D \leq 0.4\text{mm}, n \leq 4$ allow $D > 0.4\text{mm}$ is not allowed $(n \leq 8)$ items are allowed within 5 mm in diameter) </p> | MI | Visual / Microscope | Zone A |
| 11 | PCB damaged/ Poor welding/ Curl | <p>PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$</p> | MI | Visual / Ruler | Zone B |
| 12 | Edge glue height/ Edge glue bubble | <p>Edge Adhesives $H \leq$PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 0.5\text{mm}$. $n \leq 5$</p> | MI | | |
| 13 | Protect film | Surface scratch but not effect protect function, Allow | MI | Visual Inspection | Zone B |
| 14 | Silicon glue | <p>Thickness \leq PS surface(With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.</p> | MI | Visual Inspection | |
| 15 | Warp degree (TFT substrate) |  <p> $t \leq 1.5\text{mm}$ </p> | MI | Ruler | |
| 16 | Color difference in COM area (Silver point area) | Allowed | | Visual Inspection | |



13 Packaging

| | | | | | | |
|--------------------------------|--|--|--|--|----------|--|
| EPD PACKING INSTRUCTION | | | | | DATE | |
| OKRA-QS. D-010 | | | | | DESIGN | |
| | | | | | CHECKED | |
| | | | | | APPROVED | |

| | | | | | | | |
|----------|---------------|----------|-------|------------|---------|---------------|-----------|
| P/N | Customer Code | Ref. P/N | Type | PKG Method | Marking | Surface Marks | Pull Tape |
| OKRA0583 | | | GLASS | Blister | BACK | None | YES |

| Packing Materials List | | | | | 4PCS/LAYER, 20LAYER/CTN, TOTAL 80PCS/CTN. |
|------------------------|-------------------------------------|-----------|------|-------|---|
| List | Model | Materials | Q'ty | Unit | Pull tape: <div style="text-align: center; margin-top: 10px;"> </div> |
| Carton | 7# 417*362*229 mm | corrugate | 1 | Piece | |
| Inner Carton | 7#(INNER) 400*343 *95 mm | corrugate | 2 | Piece | |
| Blister | OKRA0583B PET1.0 | PET | 22 | Piece | |
| Thin foam | OKRA0583B 296.10*263.00* T1.5*1.8MM | EPE | 20 | Piece | |
| Antistatic vacuum bag | 450*590*0.075 | | 2 | Piece | |
| Foam board | OKRA2251-10 | EPE | 3 | Piece | |
| PULL TAPE | 16*5*T0.05 | | 80 | Piece | |

Detail:

Blister box:

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22

QUANTITY: 4PCS

The blister box is rotated for placement

Epaper Identification

QC: _____ PASS

Model No. _____

Quantity: _____ pcs

Date: _____

Carton No. _____ of _____



14. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| Data sheet status | |
|---|--|
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
| Product Environmental certification | |
| ROHS | |
| REMARK | |
| All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation. | |
| Transport environment | |
| When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range | |