JADARD

JD79686A

User Guide

All-in-one Driver with
TCON for Color Application

Version 1.2
2021/11/11

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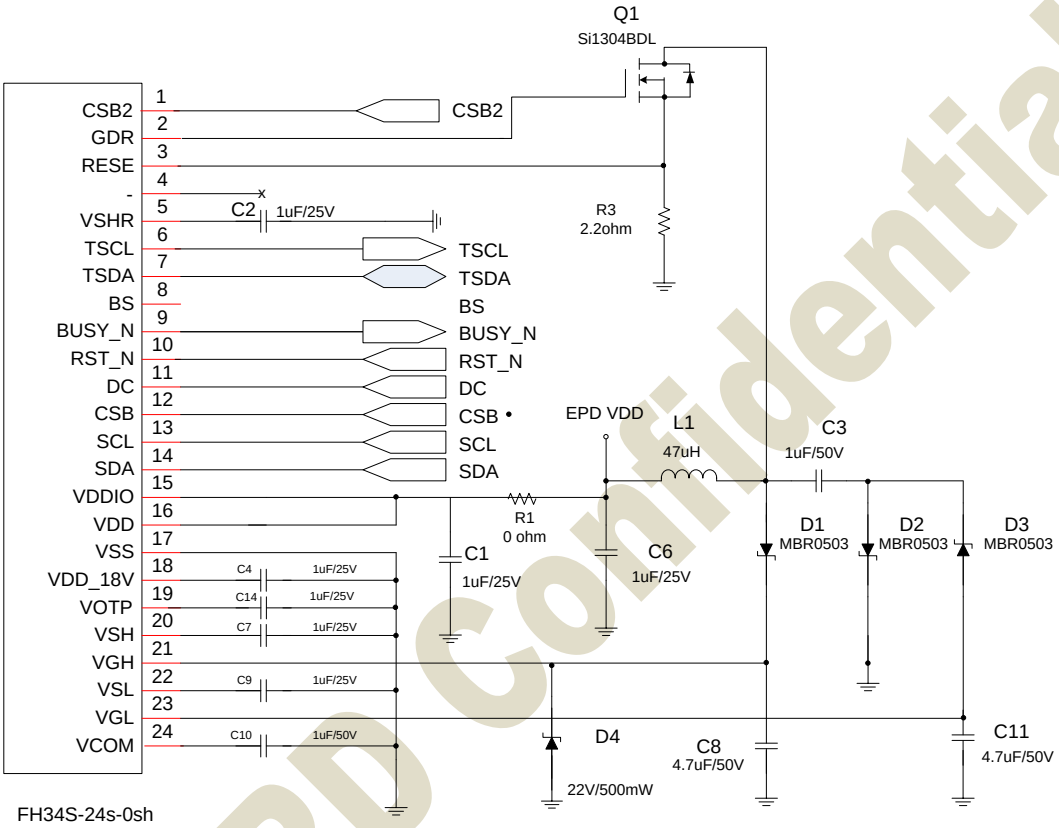
All-in-One Driver with TCON for Color Application

1. APPLICATION CIRCUIT

1.1. Power board circuit



Note:

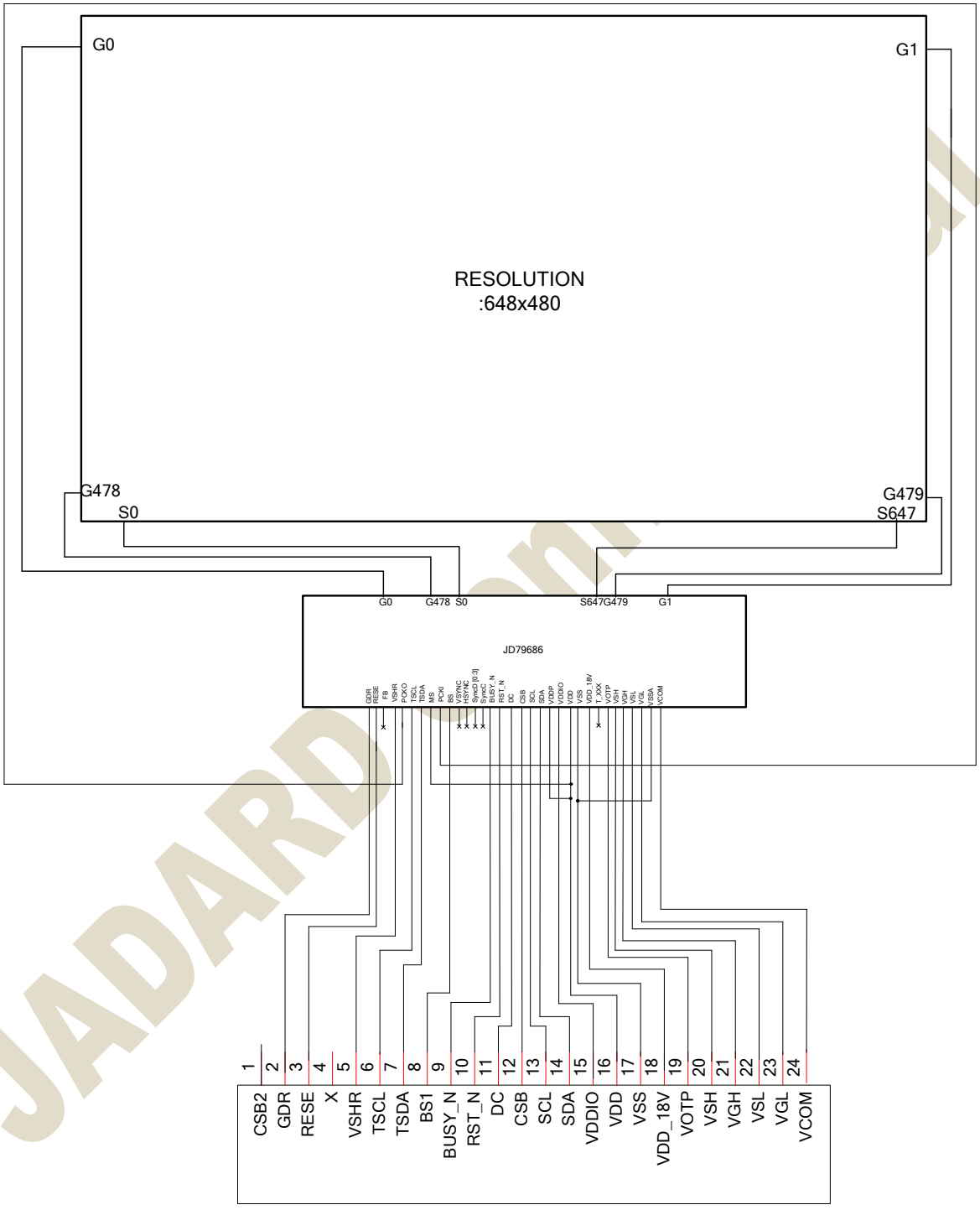
1.Power board 可共用新的及其他 compatible IC 的應用電路，搭配不同的外部電部會有相應的 boost(R06)參數需調整

2.OTP 燒錄時，建議 VOTP 需加上電容(1uF)

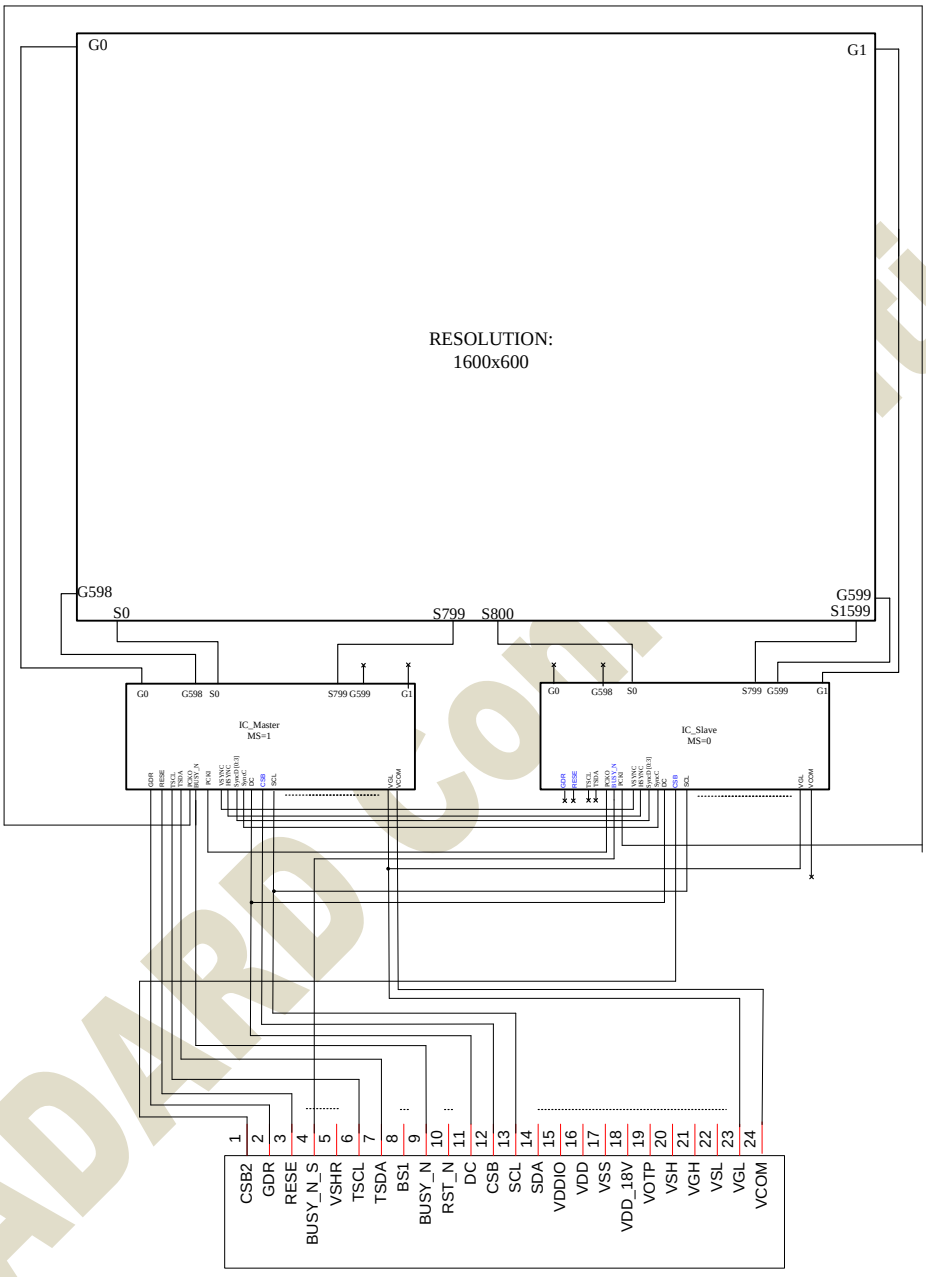
3.VGH 需加上 Zener-Diode(D4)

4.NMOS(Q1) : VDS>25V、 ID>500mA、VGS(th)<1.5V、 Ciss<200pF、RDS(on)<400mΩ

1.2. Single chip (648x480)



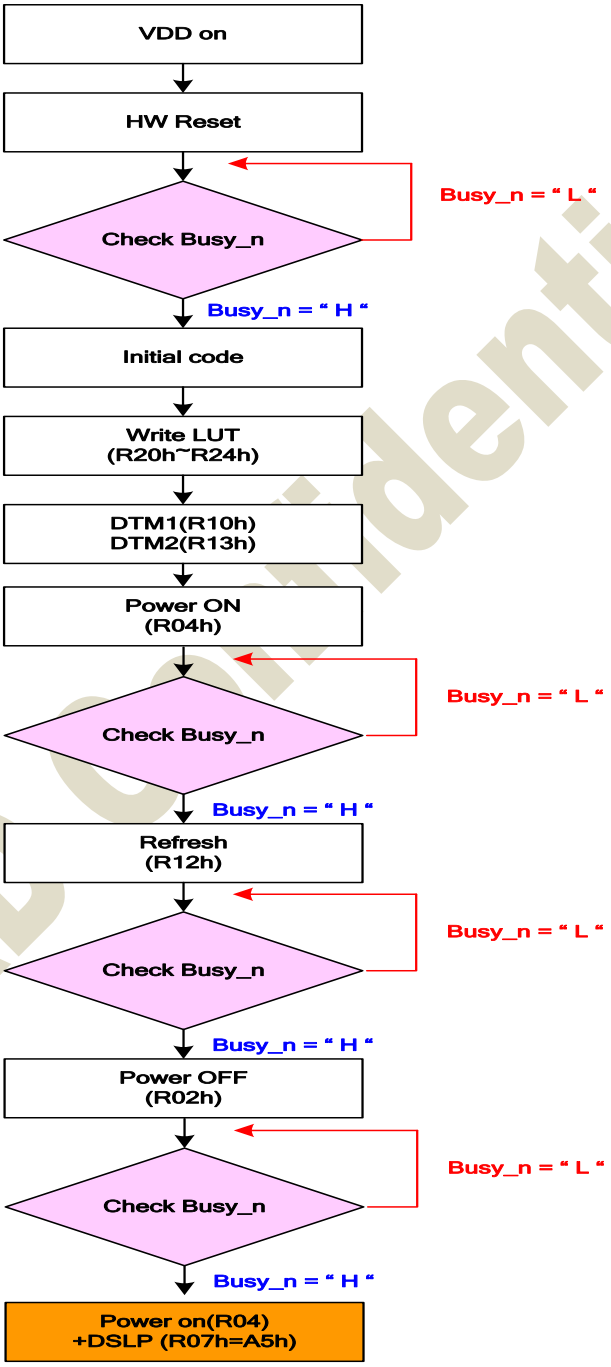
1.3. Cascade mode



Note:
1. Slave IC 的 MS 的設定為 GND
2. Slave IC 的 GDR 和 RESE 的 出 pin 需 Open，不能和 Master 相連
3. Slave IC 的 CSB 拉到 connector 的 1st pin
4. Slave IC 的 vcom 不用拉出，panel 的 VCOM 電壓由 Master 提供

2. DISPLAY FLOW

2.1 Display Flow A :T>10 度

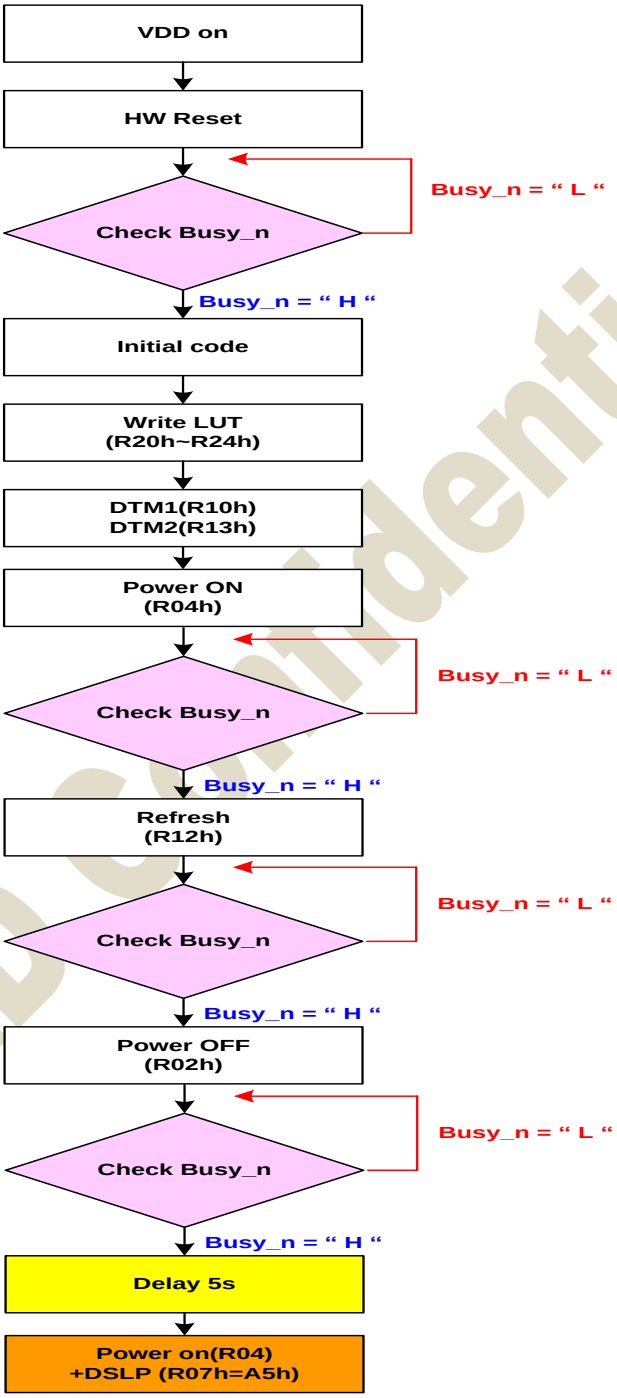


Note:

1.OTP 燒錄後的模組 display flow 不需再寫 LUT

2.進 DSLP 時，需在程序前加 power on 指令

2.2 Display Flow B :T<10 度



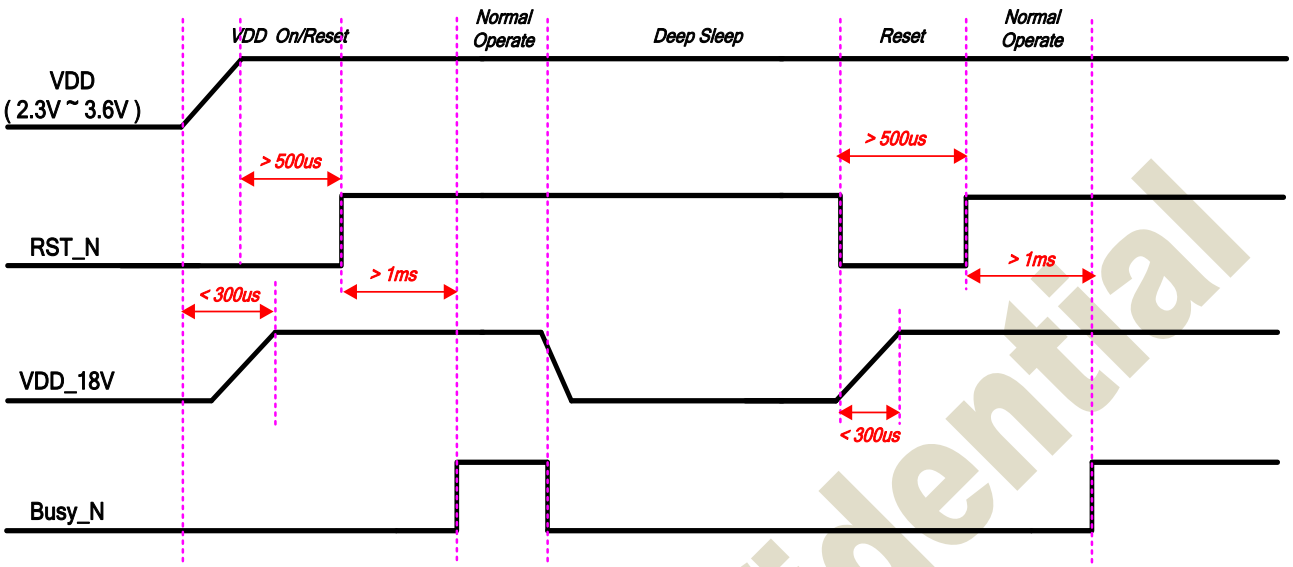
Note:

1.OTP 燒錄後的模組 display flow 不需再寫 LUT

2.10 度以下，需 delay 5S(**解低溫紅色變淡的現象**)

3.進 DSLP 時，需在程序前加 power on 指令

2.3 HW Reset



Note:

1. 重新上電後，務必作 hw reset(low->high)來作重置，確認 IC 回到最初狀態
2. Reset 後需偵測 busy_n 拉 high，來確定此時 IC 重置完成進至 normal 狀態，可以再進行其他動作
3. 進入 deep sleep mode 後，digital 電壓 VDD_18V 已關無法在下 command，如需持續操作要透過外部 hw reset(RST_N : low->high)來喚醒

2.4 Initial Code

2.4.1 Single chip

2.4.1.1 Before OTP Model

Description	Address(Hex)	Data(Hex)					Note
TDY Cmd.	08	00					Dummy code
	F8	60	A5				TDY key
	F8	93	18				停打機制關掉
	F8	73	05				調整 Vcom driving
	F8	92	08				VGL pull GND
	F8	A8	3A				r_partial_all_gate_en
	F8	88	06				Power off 時 Vcom discharge GND
User Cmd.	00	AF					黑白紅 mode/ use register
	01	3	0	3F	3F	28	電壓設定
	06	57	63	31	-	-	boost 值，需實際搭配模組再做調整
	30	3C	-	-	-	-	frame rate=50hZ
	50	57	-	-	-	-	
	61	2	88	1	E0	-	648S x 480G resolution setting
	82	2C	-	-	-	-	VCOM=-2.3V
	E8	40	-	-	-	-	Power saving
	60	04			-	-	Tcon setting
	26	0F					Group setting

2.4.1.2 After OTP Model

Description	Address(Hex)	Data(Hex)	
TDY Cmd.	08	00	-
	F8	60	A5
	F8	93	18
	F8	73	05
	F8	92	08
	F8	A8	3A
	F8	88	06

Note: 1.上述 user command 的 data 為參考值，需依實際模組狀況調整

2.各面板解析度參考設定如下:

Description	Address(Hex)	Data(Hex)				Resolution
Resolution Setting	61	3	20	1	E0	800S x 480G
	61	2	88	1	E0	648S x 480G
	61	2	80	1	E0	680S x 480G
	61	3	0	1	0	768S x 256G
	61	0	98	2	0A	152S x 522G
	61	1	18	1	E0	280S x 480G

2.4.2 Cascade mode

2.4.2.1 Master IC

Description	Address(Hex)	Data(Hex)					Note
TDY Cmd.	08	00					Dummy code
	F8	60	A5				TDY key
	F8	93	18				OSC_CLK 持續打開
	F8	73	05				調整 Vcom driving
	F8	92	08				VGL pull GND
	F8	A8	3A				r_partial_all_gate_en
	F8	88	06				Power off 時 Vcom discharge GND
User Cmd.	00	AF					黑白紅 mode/ use register
	01	3	0	3F	3F	28	電壓設定
	06	57	63	34	-	-	boost 值，需實際搭配模組再做調整
	30	3C	-	-	-	-	frame rate=50hZ
	50	57	-	-	-	-	
	61	2	88	1	E0	-	648S x 480G resolution setting
	82	2C	-	-	-	-	VCOM=-2.3V
	E8	40	-	-	-	-	Power saving
	60	04			-	-	Tcon setting
	26	0F					Group setting
	E0	01					Cascade mode

Note : For 2+2 cascade, 0xF8 = 93h, 19h

2.4.2.2 Slave IC

Description	Address(Hex)	Data(Hex)					Note
TDY Cmd.	08	00					Dummy code
	F8	60	A5				TDY key
	F8	93	18				OSC_CLK 持續打開
	F8	73	05				調整 Vcom driving
	F8	92	08				VGL pull GND
	F8	A8	3A				r_partial_all_gate_en
	F8	88	06				Power off 時 Vcom discharge GND
User Cmd.	00	AF					黑白紅 mode/ use register
	01	0	0	3F	3F	28	設定為外灌 power 模組，電壓由 Master 提供
	06	57	63	34	-	-	boost 值，需實際搭配模組再做調整
	30	3C	-	-	-	-	frame rate=50hZ
	50	57	-	-	-	-	
	61	2	88	1	E0	-	648S x 480G resolution setting
	82	2C	-	-	-	-	VCOM=-2.3V
	E8	40	-	-	-	-	Power saving
	60	04			-	-	Tcon setting
	26	0F					Group setting
	E0	01					Cascade mode

Note : For 2+2 cascade, 0xF8 = 93h, 19h

2.5 Look-UP Table (LUT)

以下 LUT waveform 為常溫簡單的例子，實際對應的 LUT waveform 需依實際模組 fine tuning；詳細參數設定內容在請參考 register description。

2.5.1 BW Mode Waveform (for R1.2 Film Application)

Name	Address(Hex)	Group 1						Group 2						Group 3					
		P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15	P16	P17	P18
LUTC	20	00	19	01	19	01	01	00	14	01	14	01	02	00	19	01	19	01	01
LUTWW	21	40	19	01	19	01	01	84	14	01	14	01	02	80	19	01	19	01	01
LUTBW	22	40	19	01	19	01	01	84	14	01	14	01	02	80	19	01	19	01	01
LUTWB	23	08	19	01	19	01	01	84	14	01	14	01	02	04	19	01	19	01	01
LUTBB	24	08	19	01	19	01	01	84	14	01	14	01	02	04	19	01	19	01	01

Name	Address(Hex)	Group 4						Group 5						Group 6					
		P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31	P32	P33	P34	P35	P36
LUTC	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTWW	21	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTBW	22	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTWB	23	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTBB	24	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Name	Address(Hex)	Group 7					
		P37	P38	P39	P40	P41	P42
LUTC	20	00	00	00	00	00	00
LUTWW	21	00	00	00	00	00	00
LUTBW	22	00	00	00	00	00	00
LUTWB	23	00	00	00	00	00	00
LUTBB	24	00	00	00	00	00	00

Note: VGH/VGL=+/-20V、VSH/VSL=+/-15V @ Frame rate=50Hz

2.5.2 BWR Mode Waveform (for R1.2 Film Application)

Name	Address (Hex)	Group 1						Group 2						Group 3					
		P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15	P16	P17	P18
LUTC	20	00	51	51	51	54	01	00	28	28	00	00	05	00	14	01	14	01	0f
LUTR	22	A8	51	51	51	54	01	80	28	28	00	00	05	48	14	01	14	01	0f
LUTW	23	90	51	51	51	54	01	10	28	28	00	00	05	48	14	01	14	01	0f
LUTB	24	90	51	51	51	54	01	80	28	28	00	00	05	48	14	01	14	01	0f

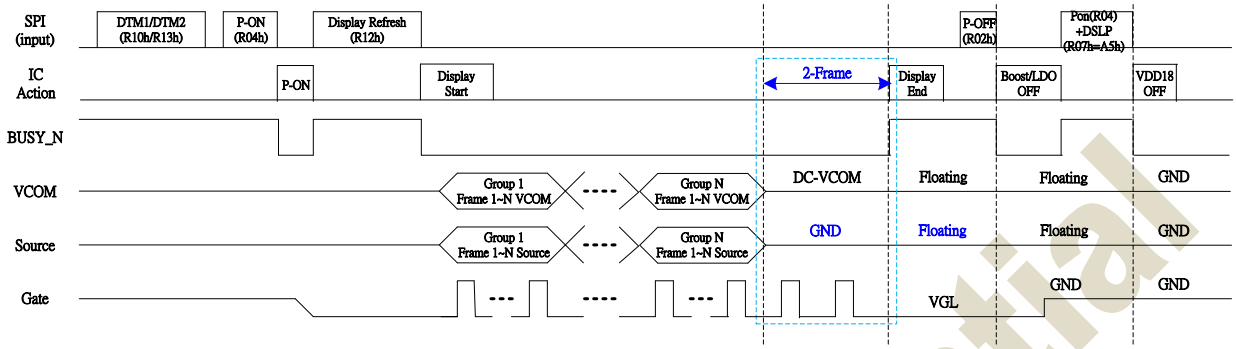
Name	Address(Hex)	Group 4						Group 5						Group 6					
		P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31	P32	P33	P34	P35	P36
LUTC	20	00	28	28	14	0	05	00	04	3c	02	1e	07	00	03	32	02	1e	04
LUTR	22	18	28	28	14	0	05	B4	04	3c	02	1e	07	B4	03	32	02	1e	04
LUTW	23	80	28	28	14	0	05	00	04	3c	02	1e	07	00	03	32	02	1e	04
LUTB	24	10	28	28	14	0	05	00	04	3c	02	1e	07	00	03	32	02	1e	04

Name	Address (Hex)	Group 7					
		P37	P38	P39	P40	P41	P42
LUTC	20	0	10	10	0	0	01
LUTR	22	F0	10	10	0	0	01
LUTW	23	0	10	10	0	0	01
LUTB	24	0	10	10	0	0	01

Note: VGH/VGL=+/-20V、VSH/VSL=+/-15V、VSHR=5V @ Frame rate=50Hz

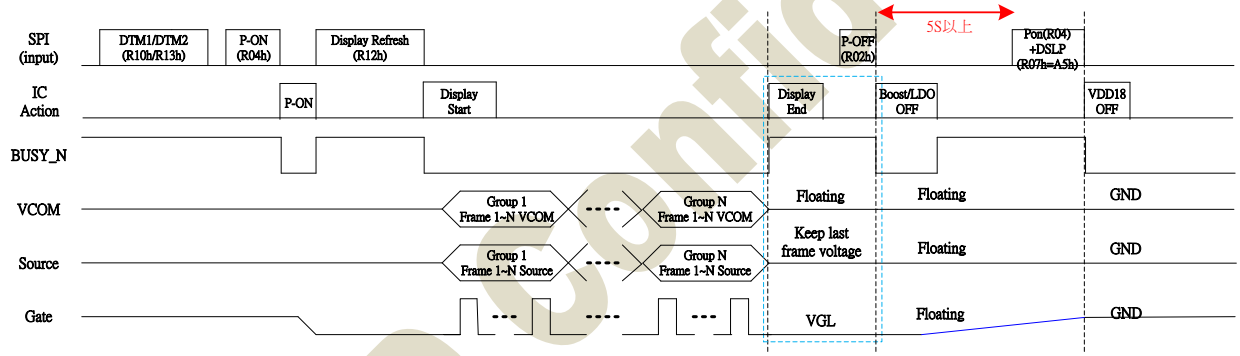
2.5.3 2-Frame ON/OFF of Source

A. 2 frame on - 針對使用在 R1.2(BWR)film 上，適用於 10℃以上設定



. B. 2 frame off - 針對使用在 R1.2(BWR)film 上，適用於 10℃以下設定

設定方式為在 display LUT 結束後，LUTC(R20h) level selection 加上"11"；並且要下 TDY command 0xF8 0x92 0x00，將 VGL 做 Hiz 的設定



2.6 Busy_N Flag

部份 cmd.執行時 busy_n 會拉 low 則 IC 進入工作狀態，工作結束時會再拉回 high；建議執行會 flag 的 cmd.時，MCU 需等 busy_n 拉 high 後再執行其他工作。

Register	Refresh restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R03H(PFS)	X	No action
R04H(PON)	X	Flag
R05H(PMES)	X	No action
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R13H(DTM2)	X	No action
R14H(PDTM1)	X	No action
R15H(PDTM2)	X	No action
R16H(PDRF)	X	Flag
R20H(LUTC)	X	No action
R21H(LUTWW)	X	No action
R22H(LUTBW/LUTR)	X	No action
R23H(LUTWB/LUTW)	X	No action
R24H(LUTBB/LUTB)	X	No action
R25H(LUTC Option)	X	No action
R26H(SET_STG)	Valid in BWR mode	No action
R30H(OSC)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R60H(TCON)	X	No action
R61H(TRES)	X	No action
R62H(TSGS)	X	No action
R70H(REV)	Valid only read	No action
R71H(FLG)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
RA0H(PGM)	X	No action
RA1H(APG)	X	Flag
RA2H(ROTP)	X	Flag
RE5H(TSSET)	X	No action
RE6H(LVSEL)	X	No action
RE7H (PBC)	Valid (only read)	Flag
RE8H (PWS)	X	No action
RE9H (AUTO):	Valid in standby	Flag
REBH	X	No action
RECH	X	Flag
REEH	X	No action
REFH	X	Flag
REFH (CHKSUM_PG)	X	No action
RF0H (RM_LUT_CMD)	X	No action
RF1H (SET_OTP_BANK)	X	No action
RF2H (RD_CHKSUM)	Valid only read	No action
RF3H (CAL_CHKSUM)	X	Flag

3. REGISTER DESCRIPTION

3.1 User command

3.1.1 R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. **(default)**
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → …→S2 →Last data=S1. 1: Shift right: First data=S1→ S2 → …→Sn-1 → Last data=Sn. **(default)**
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→ G2 → Last line=G1. 1:Scan up; First line=G1 →G2 →…→Gn-1 →Last line=Gn. **(default)**
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. **(default)** 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP**(default)** 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 600x448 01: Display resolution is 640x480 10: Display resolution is 720x540 11: Display resolution is 800x600 (default)

Notes:

1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.

2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

3.1.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1	-	-	-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
5th Parameter	W	1	-	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	**Gate power selection.** 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	**Source power selection.** 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL. (default)

2nd Parameter:

Bit	Name	Description
2-0	VGHL_LV	**VGHL_LV Voltage Level.** 000: VGH=20 v, VGL=-20v (default) 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v 110: VGH=14 v, VGL=-14v 111: VGH=13 v, VGL=-13v
3	VCOM_HV	**VCOM Voltage Level** 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC(default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT. **(Default value: 111111b)**

Bit	Name	Description
5-0	**VSH**	**Internal VSH power selection.** 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v ….

		010111: 7.0V 011000: 7.2 V 011001: 7.4 V …. 111010: 14.0V 111011: 14.2 V 111100: 14.4V 111101: 14.6V 111110: 14.8V 111111: 15.0V

4th Parameter: Internal VSL power selection for B/W LUT. **(Default value: 111111b)**

Bit	Name	Description
5-0	**VSL**	**Internal VSL power selection.** 000000: -2.4 v 000001: -2.6 v 000010: -2.8 v 000011: -3.0 v …. 010111: -7.0V 011000: -7.2 V 011001: -7.4 V …. 111010 :-14.0V 111011: -14.2 V 111100: -14.4 V 111101: -14.6V 111110: -14.8V 111111: -15.0V

5th Parameter: Internal VSHR power selection for Red LUT. **(Default value: 00001111b)**

Bit	Name	Description
6-0	**VSHR**	**Internal VSL power selection.** 0000000: 2.4 v 0000001: 2.5 v 0000010: 2.6 v 0000011: 2.7 v …. 0101110: 7.0 V 0101111: 7.1 V 0110000: 7.2 V …. 1010001: 10.5V 1010010: 10.6 V 1010011: 10.7 V 1010100: 10.8V 1010101: 10.9V 1010110: 11.0V

Note:
1.VSH>VSHR

Restriction	

3.1.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will keep floating.
Restriction	

3.1.4 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.
Restriction	

3.1.5 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	

3.1.6 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
2nd Parameter	W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
3rd Parameter	W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	**Driving strength of phase A**	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase A**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	**Driving strength of phase B**	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase B**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

Description	3rd Parameter: Bit / Name / Description 2-0 / **Minimum OFF time setting of GDR in phase C** / 000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8 5-3 / **Driving strength of phase C** / 000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
Restriction	

3.1.7 R07H (DSLP): Deep Sleep

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	

3.1.8 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

3.1.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1".

3.1.10 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

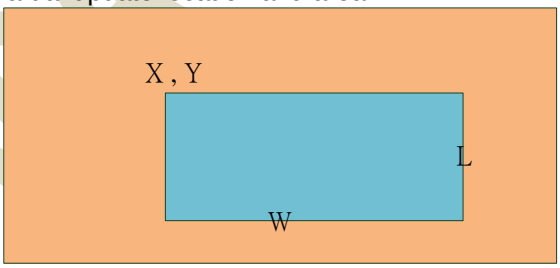
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

3.1.11 R14H (PDTM1): Partial Data Start transmission 1 Register

R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

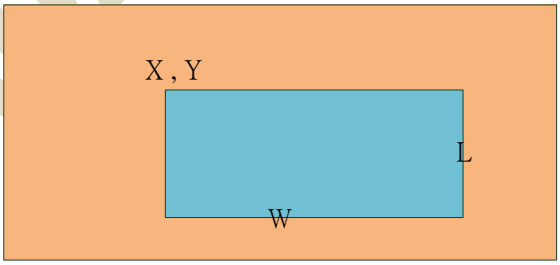
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

3.1.12 R15H (PDTM2): Partial Data Start transmission 2 Register

R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	0	15H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

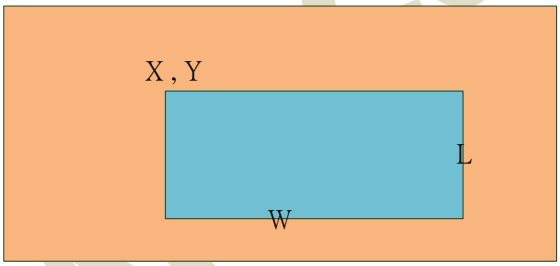
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

3.1.13 R16H (PDRF): Partial Display Refresh Command

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	DFV_EN						X[9]	X[8]	00h
2nd Parameter			X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter	W	1							Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	00h
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	
8th Parameter			L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT After display refresh command, BUSY_N signal will become "0".  Note: X and W should be the multiple of 8. DFV_EN: data follow VCOM function on display area. DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT. DFV_EN=0: Data doesn't follow VCOM LUT.
Restriction	this command only active when BUSY_N = "1".

3.1.14 R20H (LUTC): LUT for Vcom

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~13th Parameter	W	1	2nd state								00h
….	W	1	3rd ~9th state								00h
55th ~60h Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT. This command stores VCOM Look-Up Table with 10 states of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.
Restriction	- This command only actives when BUSY_N = "1".

define	description
Level selection [1:0]	00: -VCM_DC 01: VSH+VCM_DC. 10: VSL+VCM_DC. 11: Floating.
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame … 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 00000001: 1 … 11111110: 254 11111111: 255

3.1.15 R21H (LUTWW): White to White LUT Register

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	1	21H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.
Restriction	- This command only actives when BUSY_N = "1".

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

3.1.16 R22H (LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~9th state								00h
55th ~60th Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.
Restriction	- This command only actives when BUSY_N = "1".

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

3.1.17 R23H (LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

3.1.18 R24H (LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

3.1.19 R25H (LUTC Option): LUTC option

R25H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC option	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1							XON [9:8]		00h
2nd Parameter	W	1	XON [7:0]								00h
3rd Parameter	W	1							VCOM_H [9:8]		00h
4th Parameter	W	1	VCOM_H [7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

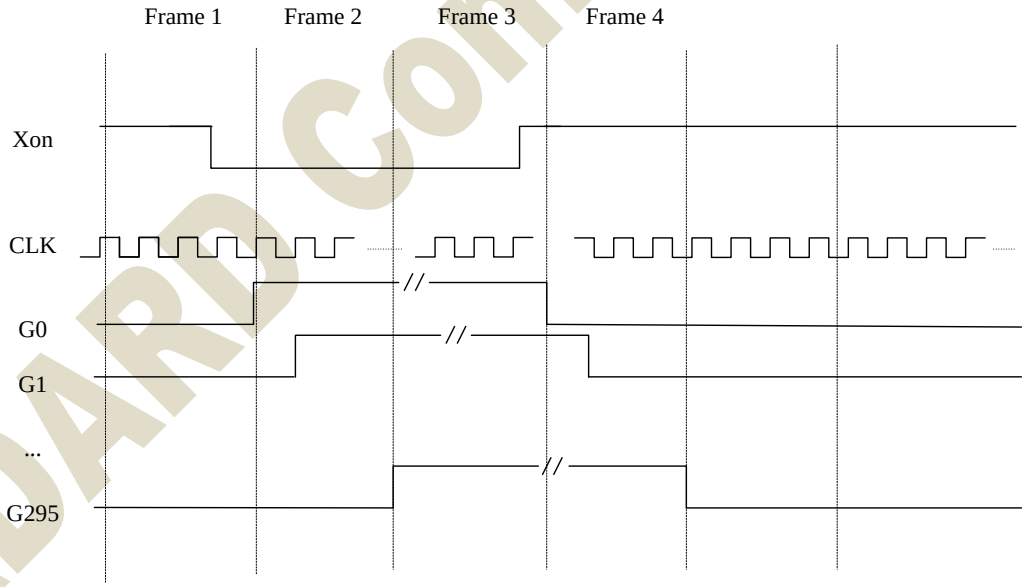
Description

-The command defines as:

This register is set for VCOM LUT.

XON[9:0]	All Gate ON 0000000000: No all gate on. 0000000001: State1 gate power on 1111111111: State1~10 all gate power on
VCOM_H[9:0]	Control VCOM Power as High 0000000000: No VCOM High voltage 0000000001: State1 VCOM High voltage …. 1111111111: State1~10 VCOM High voltage

Xon function:



Restriction

- This command only actives when BUSY_N = "1".

3.1.20 R26H (SET_STG): Set VCOM/Red States

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_STG	W	0	0	0	1	0	0	1	1	0	H
1st Parameter	W	1			-	-	vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h

Description	This command is used to set VCOM/Red LUT states Function of vcom_stg_sel [1:0]/ b2w_stg_sel[1:0] are shown below Value / Stages 00 / 7 01 / 8 10 / 9 11 / 10 Default is set as 7 stages.
Restriction	These settings are valid for BWR mode.

3.1.21 R30H (OSC): OSC control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OSC	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: "-" Don't care, can be set to VDD or GND level

Description

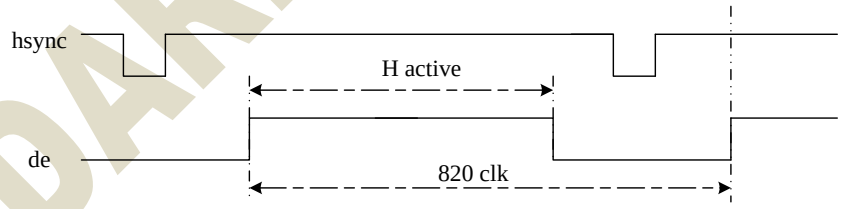
-The command defines as:

The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

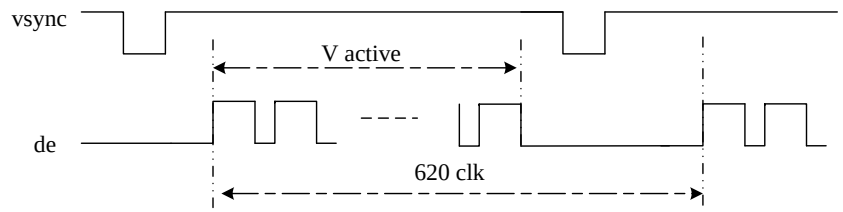
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ (default)
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction

3.1.22 R40H (TSC): Temperature Sensor Command

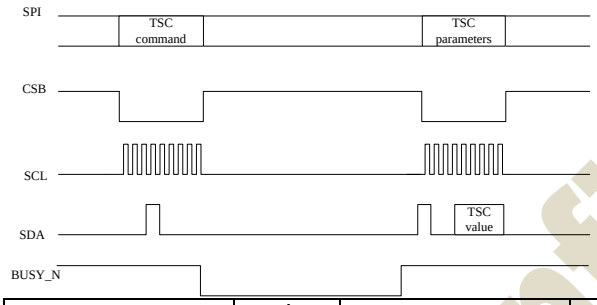
R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2	D1	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction

This command only actives after R04H(PON) or R05H(PMES)

3.1.23 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the driver IC temperature sensor enable and calibration function. **Bit** / **temperature** 2-0: mean temperature offset value 000:0℃ 001:1℃ 010:2℃ …. 111:7℃ 3: Positive and negative value 0:"+" 1: "-" 7: **Internal temperature sensor enable** 0: Internal temperature sensor enable.(**default**) 1: Internal temperature sensor disable, using external temperature sensor. For example: 1100: - 4 degree c 0111: + 7 degree c
Restriction	This command only actives after R04H(PON) or R05H(PMES)

3.1.24 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

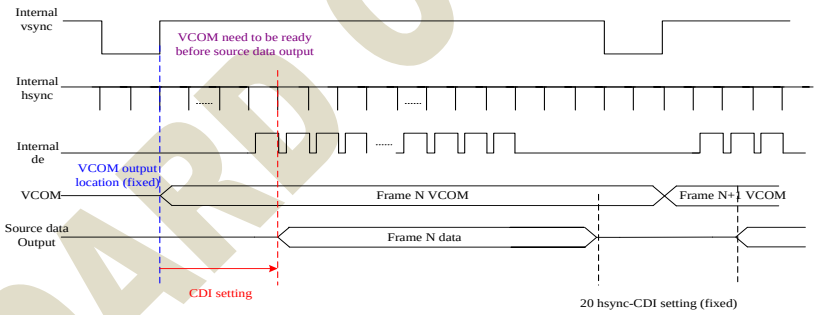
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	
3-0	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0] Border data selection.

B/W/Red mode(BWR=0)

Bit 5-4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 5-4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (1->0)
	10	LUTBW (0->1)
	11	Floating

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)

Bit 5-4	Description	
DDX[1:0]	Data (Red, B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

Bit 5-4	Description	
DDX[0]	Data (New,Old)	LUT
0	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
1 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

3.1.25 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE6H (LVSEL)). 1st Parameter:
Restriction	

Bit 0	LPD
0	Low power input.
1	Normal status.

3.1.26 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	00h

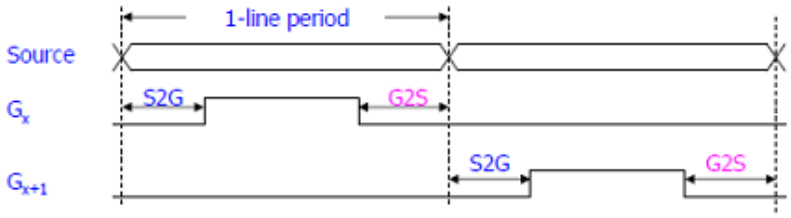
NOTE: "-" Don't care, can be set to VDD or GND level

Description

- The command define Non-overlap period of gate and source as below:
  1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 2 clock(default) 0001: 4 clock 0010: 6 clock 0011:8 clock 0100: 10 clock 0101: 12 clock 0110: 14 clock 0111: 16 clock 1000: 18 clock 1001: 20 clock 1010: 22 clock 1011: 24 clock 1100: 26 clock 1101: 28 clock 1110: 40 clock 1111: 32 clock

Period=660ns



1 line times=1 frame times/620 line(max.gate(600 lines)+fix blanking(20 lines)
Gate on time= 1 line times-gate off time(S2G+G2S times)

Restriction

3.1.27 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1							HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
3th Parameter	W	1							VRES(9)	VRES(8)	ooh
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution = HRES Vertical display resolution = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127)
Restriction	

3.1.28 R62H (TSGS): Source & gate start setting

R62H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSGS	W	0	0	1	1	0	0	0	1	0	62H
1st Parameter	W	1							S_Start (9)	S_Start (8)	00h
2nd Parameter	W	1	S_Start (7)	S_Start (6)	S_Start (5)	S_Start (4)	S_Start (3)	-	-	-	00h
3th Parameter	W	1				gscan			G_Start (9)	G_Start (8)	ooh
4th Parameter	W	1	G_Start (7)	G_Start (6)	G_Start (5)	G_Start (4)	G_Start (3)	G_Start (2)	G_Start (1)	G_Start (0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

3.1.29 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from OTP address = 0x001.& 0x002
Restriction	- This command only actives when BUSY_N = "1".

3.1.30 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80 H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function
0	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

Restriction

This command only actives when BUSY_N = "1".

3.1.31 R81H (VV): Vcom Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command could get the Vcom value 1st Parameter: Bit: 5-0 Function: Vcom value 000000: -0.1V 000001:-0.15V 000010:-0.2V …. 111000:-2.9V 111001:-2.95V 111010:-3.0V
Restriction	This command only actives when BUSY_N = "1".

3.1.32 R82H (VDCS): Vcom_DC Setting register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1st Parameter:

Bit	Function
5-0	**VCOM value** 000000: -0.1V 000001:-0.15V 000010:-0.2V …. 111000:-2.9V 111001:-2.95V 111010:-3.0V

Restriction	This command only actives when BUSY_N = "1".

3.1.33 RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.
Restriction	This command only actives when BUSY_N = "1".

3.1.34 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

NOTE: "-" Don't care, can be set to VDD or GND level

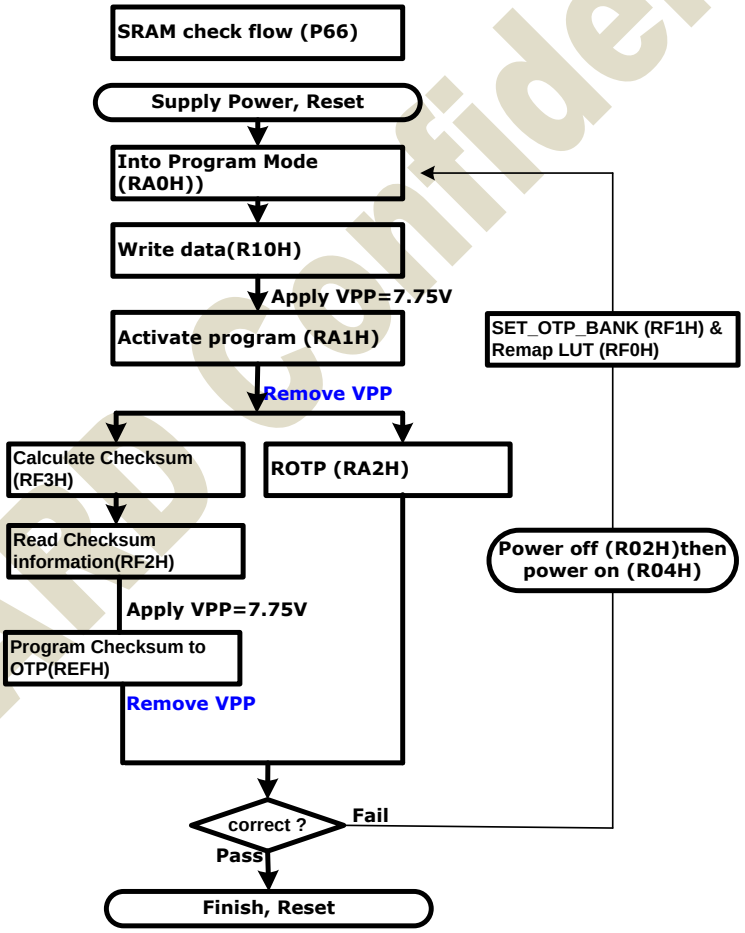
Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

3.1.35 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~ (m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.
Restriction	This command only actives when BUSY_N = "1".



The sequence of programming OTP

3.1.36 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter:

Bit	
0	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
1	Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.

Restriction	This command only actives when BUSY_N = "1".

3.1.37 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to fix the temperature value of master and salve
Restriction	

3.1.38 RE7H (PBC): Panel Break Check

RE7H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	1	E7H
1st Parameter	R	1								PSTA	-

Description	This command is used to enable panel check, and to disable after reading result. 1st Parameter:

Bit	PSTA
0	Panel check fail (panel broken).
1	Panel check pass

Restriction	

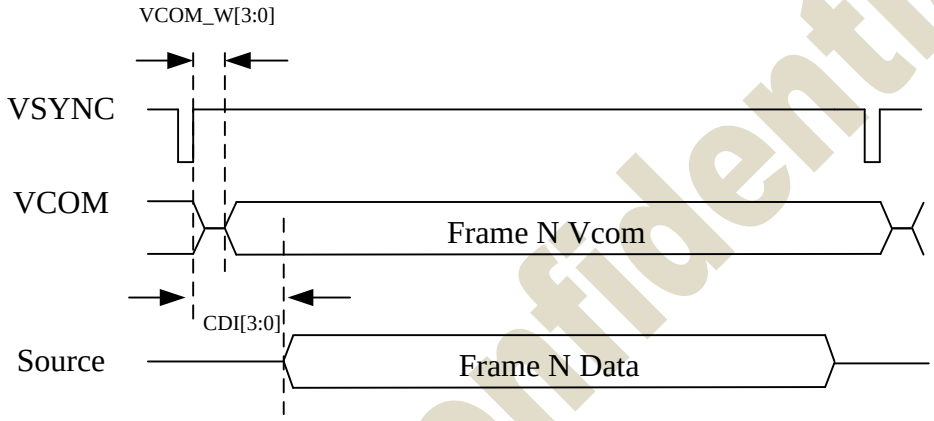
3.1.39 RE8H (PWS): Power Saving

RE8H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Power Saving	W	0	1	1	1	0	1	0	0	0	E8H
1st Parameter	W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h

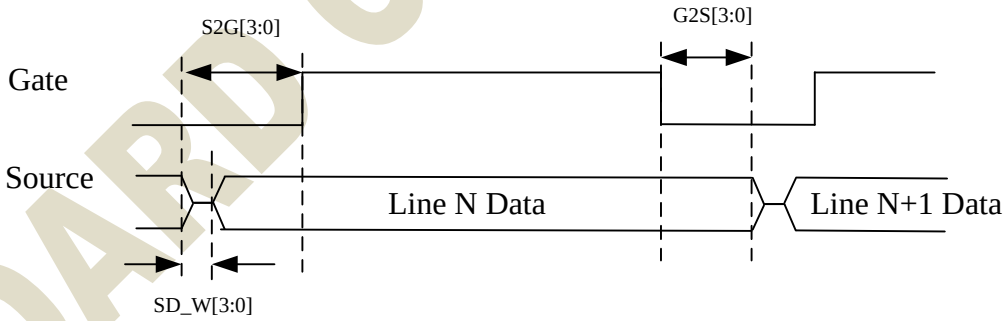
Description

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.1st Parameter:

Vcom_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



Restriction

3.1.40 RE9H (AUTO): AUTO Sequence

RE9H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AUTO Sequence	W	0	1	1	1	0	1	0	0	1	E9H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	00h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0xE9) + Code(0xA5) = (PON->DRF->POF) AUTO (0xE9) + Code(0xA7) = (PON->DRF->POF->DSLP)
Restriction	

`

3.1.41 RF1H (SET_OTP_BANK): Set OTP program bank

RF1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	1	0	0	0	1	F1H
1st Parameter	W	1			-	-	-	-	LUT_bank0	reg_bank0	03h

Description

This command is used to set program bank for registers and LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h~BFFh	LUTs	D00h~17FFh	LUTs

reg_bank :

Value	Function
1	Program “Temp. segment” and “Default Setting” in bank 0
0	Program “Temp. segment” and “Default Setting” in bank 1

LUT_bank :

Value	Function
1	Program “LUTs” in bank 0
0	Program “LUTs” in bank 1

Restriction

3.2 TDY Command

TDY command 為 IC 內部相關功能控制的 register；

W/R	Address (Hex)	Data (Hex)		Description
W	F8	60	A5	Enter TDY cmd.
W	F8	73	05	調整 AC vcom 時的 VCOM driving 能力
W	F8	92	08	Power off 時 VGL 拉到 GND (10 度以上)
		92	00	Power off 時 VGL Hiz(10 度以下)
W	F8	A8	3A	Partial 區外的 gate 全開
		A8	32	關閉上述功能
W	F8	93	18	Osc clock 不停止
		93	1A	Osc clock 停止
W	F8	88	06	Power off 時 Vcom discharge GND
		88	02	Power off 時 Vcom Hiz
W	F8	B8	80	Vcom initial setting VCOM DC
		B8	A0	Vcom initial setting VCOM Hiz
W	F8	7E	31	Boost mode:constant on time
		7E	01	Boost mode: current mode

Note:

1. 使用 TDY cmd.前皆需先下 0xF8 = 60h A5h 後方可使用，相關內容可參考上表
2. 有顏色標註部份建議在 initial code 就加入
3. 0x92 的設定在 10 度以上和以下的設定不同，請在 MCU 作設定
4. TDY cmd.需放於 user cmd.前面，需 follow 下圖的下 code 順序，並且最前面需要先下一個 0x08 = 00h 的 dummy code

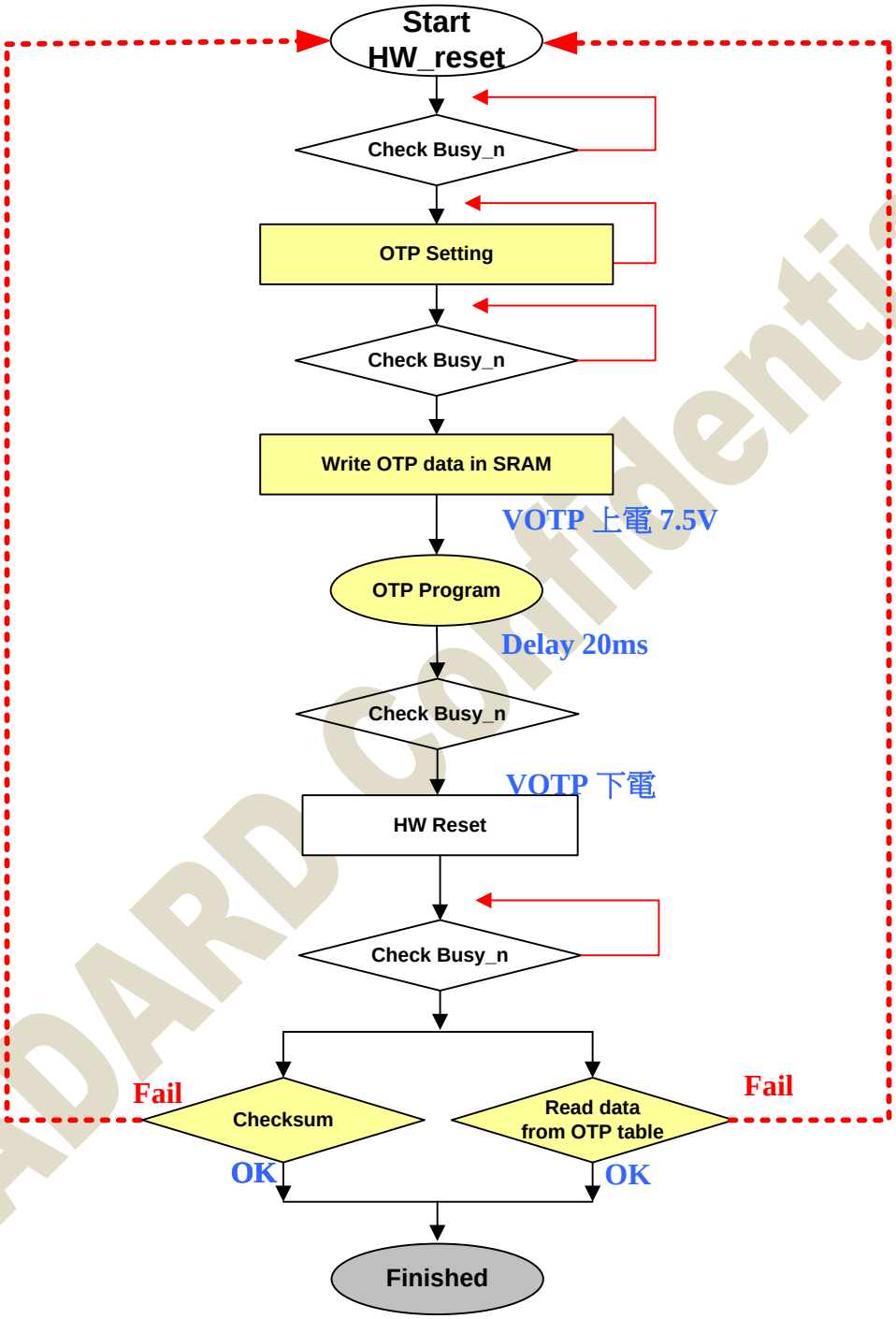
```
EPD_W21_WriteCMD(0x08);           //dummy code 避免 f8的code吃不到
EPD_W21_WriteDATA (0x00);

EPD_W21_WriteCMD(0xF8);           //解鎖
EPD_W21_WriteDATA (0x60);
EPD_W21_WriteDATA (0xA5);

EPD_W21_WriteCMD(0xF8);            //OSC不停打
EPD_W21_WriteDATA (0x93);
EPD_W21_WriteDATA (0x18);


EPD_W21_WriteCMD(0x01);                 //POWER SETTING
        EPD_W21_WriteDATA (0x03);
        EPD_W21_WriteDATA (0x00);
        EPD_W21_WriteDATA (0x3F);
        EPD_W21_WriteDATA (0x3F);              // 15V
```

3.3 IC Vender ID Read

W/R	Address (Hex)	Data (Hex)	Description
W	F8	C7	
R	F9	XX	讀取 0xC7 會得到 Vender_ID: **61**

4. OTP FLOW AND CONTENT

4.1 Single mode OTP Flow



4.1.1 OTP Setting

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
F0	1	2	W	1 F, 1 F	User TR0~TR8+Backup1/2 : rF0=0F, 0F User TR0~TR9 + Backup1 : rF0=0F, 1F User TR0~TR10 : rF0=1F, 1F
A0	1	1	W	A5	PG MODE

4.1.2 Write OTP data in SRAM

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
10	1	3072	W		寫入欲燒入的 OTP data

4.1.3 OTP Program

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
A1	0	0	W	-	APG

4.1.4 Read data from OTP table

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
A2	1	3073 or 6145	R		檢查 OTP 是否有燒錄成功 : - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P255 為 TDY 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3168~P3327 為 TDY 使用，可忽略)

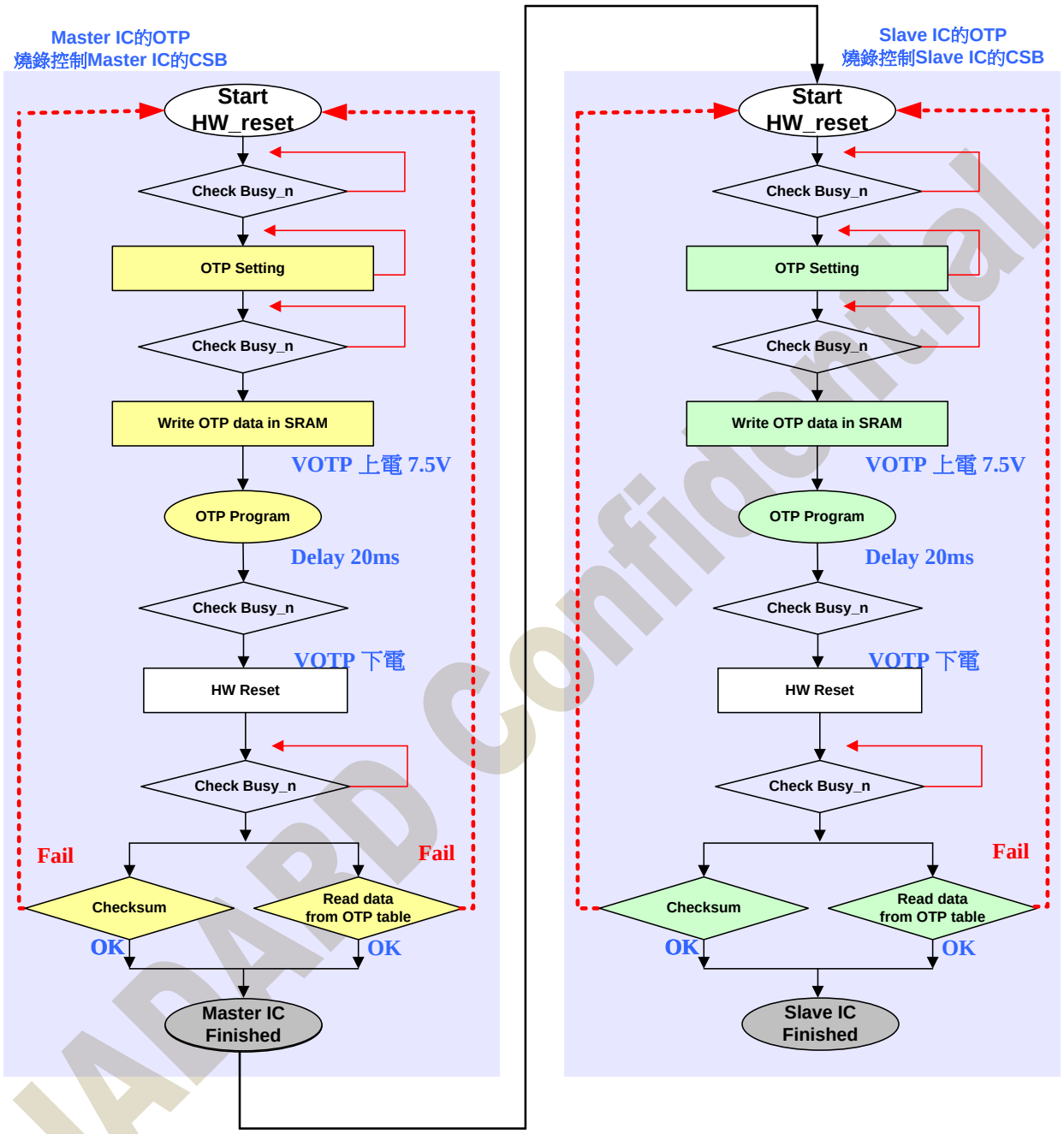
4.1.5 Checksum

Address	Start addr.	Counts	R/W	Data	Comment
F3	0	0	W		計算 OTP checksum
F2	1	13	R		Read checksum value

Note:

1. 若需節省 OTP 回讀時間，可以使用 check sum 的方式做資料比對
2. Check sum 比對資料為各溫段的 LUT 資料

4.2 Cascade mode OTP flow



4.2.1 Master Setting

OTP Setting

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
F0	1	2	W	1 F, 1 F	User TR0~TR8+Backup1/2 : rF0=0F, 0F User TR0~TR9 + Backup1 : rF0=0F, 1F User TR0~TR10 : rF0=1F, 1F
A0	1	1	W	A5	PG MODE

Write OTP data in SRAM

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
10	1	3072	W		寫入欲燒入的 Mater OTP data

OTP Program

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
A1	0	0	W	-	APG

Read data from OTP table

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
A2	1	3073 or 6145	R		檢查 OTP 是否有燒錄成功 : - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P255 為 TDY 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3168~P3327 為 TDY 使用，可忽略)

Checksum

Address	Start addr.	Counts	R/W	Data	Comment
F3	0	0	W		計算 OTP checksum
F2	1	13	R		Read checksum value

Note:

1. 若需節省 OTP 回讀時間，可以使用 check sum 的方式做資料比對
2. Check sum 比對資料為各溫段的 LUT 資料
3. Master 和 Slave IC 的 OPT data 會有差異，參考 initial code 的差異，分別填入相對應的值

4.2.2 Slave Setting

OTP Setting

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
F0	1	2	W	1 F, 1 F	User TR0~TR8+Backup1/2 : rF0=0F, 0F User TR0~TR9 + Backup1 : rF0=0F, 1F User TR0~TR10 : rF0=1F, 1F
A0	1	1	W	A5	PG MODE

Write OTP data in SRAM

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
10	1	3072	W		寫入欲燒入的 Slave OTP data

OTP Program

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
A1	0	0	W	-	APG

Read data from OTP table

Address (Hex)	Start Addr.	Counts	R/W	Data (Hex)	Comment
A2	1	3073 or 6145	R		檢查 OTP 是否有燒錄成功 : - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P255 為 TDY 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3168~P3327 為 TDY 使用，可忽略)

Checksum

Address	Start addr.	Counts	R/W	Data	Comment
F3	0	0	W		計算 OTP checksum
F2	1	13	R		Read checksum value

Note:

1. 若需節省 OTP 回讀時間，可以使用 check sum 的方式做資料比對
2. Check sum 比對資料為各溫段的 LUT 資料
3. Master 和 Slave IC 的 OPT data 會有差異，參考 initial code 的差異，分別填入相對應的值

4.2 OTP Content

OTP bank 0 (3K bytes)		OTP bank 1 (3K bytes)	
Address(Hex)	Content	Address(Hex)	Content
0x000	otp_chk (A5)	0xC00	otp_chk (A5)
0x001	otp_ver [7:0]	0xC01	otp_ver [7:0]
0x002	otp_ver [15:8]	0xC02	otp_ver [15:8]
0x003	otp_temp0	0xC03	otp_temp0
0x004	otp_temp1	0xC04	otp_temp1
0x005	otp_temp2	0xC05	otp_temp2
0x006	otp_temp3	0xC06	otp_temp3
0x007	otp_temp4	0xC07	otp_temp4
0x008	otp_temp5	0xC08	otp_temp5
0x009	otp_temp6	0xC09	otp_temp6
0x00A	otp_temp7	0xC0A	otp_temp7
0x00B	otp_temp8 (optional)	0xC0B	otp_temp8 (optional)
0x00C	otp_temp9 (optional)	0xC0C	otp_temp9 (optional)
0x00D ~ 01F	Reserved	0xC0D ~ C1F	Reserved
0x020~0x05F	Default setting	0xC20~0xC5F	Default setting
0x60~0xFF	TDY command	0xC60~0xCFF	TDY command
0x100~0x1FF	TR0 WF	D00h	TR0 WF
0x200h~0x2FF	TR1 WF	E00h	TR1 WF
0x300h~0x3FF	TR2 WF	F00h	TR2 WF
0x400h~0x4FF	TR3 WF	1000h	TR3 WF
0x500h~0x5FF	TR4 WF	1100h	TR4 WF
0x600h~0x6FF	TR5 WF	1200h	TR5 WF
0x700h~0x7FF	TR6 WF	1300h	TR6 WF
0x800h~0x8FF	TR7 WF	1400h	TR7 WF
0x900h~0x9FF	TR8 WF	1500h	TR8 WF
0xA00h~0xAFF	TR9 WF / Backup 1	1600h	TR9 WF / Backup 1
0xB00h~0xBFF	TR10 WF / Backup 2	1700h	TR10 WF / Backup 2

OTP reload key 需設“A5”

Description	OTP Address	Note
Temp.	0x000 ~ 0x00C	0x000 = A5
LUT	0x100 ~ 0xBFF	此區域沒有用到的溫段 LUT 位置皆填入 FF
User Cmd	0xAED ~ 0xB5F	OTP data 需注意以下填入值 : 1. 0x20=A5 2. Rserved 需填入 FF=>0x0D~0x1F、0x2B、 0x2F~0x32、0x42、0x4A & 0x4E~0x5F 4. 0xB49 ~ 0xB4D 如為 single chip 此處也填 FF
TDY Cmd	0x60 ~ 0xFF	此區域 OTP data 全部填入 FF (0xF1~0xFD=>checksum 保留區)

Note:

1.燒錄 bank0 時，0x000 OTP data 需設定為 A5；燒錄 bank1 時，0xC00 OTP data 需設定為 A5

2. otp_temp N-1 ＜ TR N ≦ otp_temp N ＜ TR N+1 ≦ otp_temp N+1

(ex: otp_temp4=20 度、otp_temp5=25 度 T-sensing 溫度為 21 度~25 度，此時會去抓 TR5 WF)

4.2.1 LUT setting

5R0~10 WF is the same as TR0 defined as below:

	Discription	Addr (dec)	Addr (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PS1
TR0 WF	Voltage	256	100			M[2:0]			N[2:0]			
		257	101			vsh[5:0]						
		258	102			vsl[5:0]						
		259	103		vshr[6:0]							
		260	104			vdcs[5:0]						
		261	105		vghl_lv[2:0]					XON[9:8]		
		262	106	XON[7:0]								
		263	107							VCOMH[9:8]		
		264	108	VCOMH[7:0]								
	LUTC	265	109	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		266	10A	1st Frame number[7:0]								
		267	10B	2nd Frame number[7:0]								
		268	10C	3rd Frame number[7:0]								
		269	10D	4th Frame number[7:0]								
		270	10E	Repeat number[7:0]								
		271	10F	Stage 2 ~ Stage 10								
		324	144									
	LUTWW	325	145	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		326	146	1st Frame number[7:0]								
		327	147	2nd Frame number[7:0]								
		328	148	3rd Frame number[7:0]								
		329	149	4th Frame number[7:0]								
		330	14A	Repeat number[7:0]								
		331	14B	Stage 2 ~ Stage 7								
		366	16E									
	LUTBW / LUTR	367	16F	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		368	170	1st Frame number[7:0]								
		369	171	2nd Frame number[7:0]								
		370	172	3rd Frame number[7:0]								
		371	173	4th Frame number[7:0]								
		372	174	Repeat number[7:0]								
		373	175	Stage 2 ~ Stage 10								
		426	1AA									
	LUTWB / LUTW	427	1AB	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		428	1AC	1st Frame number[7:0]								
		429	1AD	2nd Frame number[7:0]								
		430	1AE	3rd Frame number[7:0]								
		431	1AF	4th Frame number[7:0]								
		432	1B0	Repeat number[7:0]								
		433	1B1	Stage 2 ~ Stage 7								
		468	1D4									
	LUTBB / LUTB	469	1D5	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		470	1D6	1st Frame number[7:0]								
		471	1D7	2nd Frame number[7:0]								
		472	1D8	3rd Frame number[7:0]								
		473	1D9	4th Frame number[7:0]								
		474	1DA	Repeat number[7:0]								
		475	1DB	Stage 2 ~ Stage 7								
		510	1FE									

4.2.2 Default Setting

OTP reload key 需設"A5"

	32	020	Enable OTP Setting (0xA5)							value
R00H	33	021	res[1:0]		reg_en	bwr	ud	shl	shd_n	rst_n	8F
R01H	34	022							Vdg_en	Vds_en	03
	35	023						Vghl_lv[2:0]			00
	36	024			Vsh[5:0]						3F
	37	025			Vsl[5:0]						3F
	38	026		VSHr[6:0]							0F
R03H	39	027			Vsh_off[1:0]		Vsl_off[1:0]		vshr_off[1:0]		00
R06H	40	028	bt_pha[7:0]								17
	41	029	bt_phb[7:0]								17
	42	02A			bt_phc[5:0]						17
R16H	43	02B	DFV_EN	Reserved							00
--	44	02C	Reserved								FF
RE6H	45	02D							LVD_SEL[1:0]		11
RE8H	46	02E			VCOM_W[2:0]			SD_W[2:0]			00
--	47 ~ 50	02F ~ 032	Reserved								FF
R30H	51	033			M[2:0]			N[2:0]			3C
R41H	52	034	tse				To[3:0]				00
R42H	53	035	Wattr[7:0]								00
	54	036	Wmsb[7:0]								00
	55	037	Wlsb[7:0]								00
R50H	56	038	vbd[1:0]		ddx[1:0]		cdi[3:0]				D7
R60H	57	039	s2g[3:0]				g2s[3:0]				00
R61H	58	03A	Reserved						hres[9]	hres[8]	00
	59	03B	hres[7:3]								00
	60	03C							vres[9]	vres[8]	00
	61	03D	vres[7:0]								00
R80H	62	03E			amvt[1:0]		xon	amvs	amv		10
R82H	63	03F	vdcs[6:0]								1D
RE0H	64	040					cce_sel	cce_lr	tsfix	ccein	00
RE5H	65	041	ts_set[7:0]								00
R62H	66	042	Reserved						sstart[9]	sstart[8]	00
	67	043	sstart[7:3]								00
	68	044				gscan			gstart[9]	gstart[8]	00
	69	045	gstart[7:0]								00
RF0H	70	046				tr10_lut_en	rmp2_table_sel				1F
	71	047				tr9_lut_en	rmp1_table_sel				1F
RF1H	72	048							LUT_bank0	reg_bank0	03
Slave setting											
R00H	73	049	slv_res[1:0]		slv_reg_en	slv_bwr	slv_ud	slv_shl		slv_rst_n	00
R62H	74	04A	Reserved								00
	75	04B	slv_sstart[7:3]								00
	76	04C				slv_gscan			slv_gstart[9]	slv_gstart[8]	00
	77	04D	slv_gstart[7:0]								00
	78	04E	Reserved								FF
R26H	79	04F					vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00

Note:

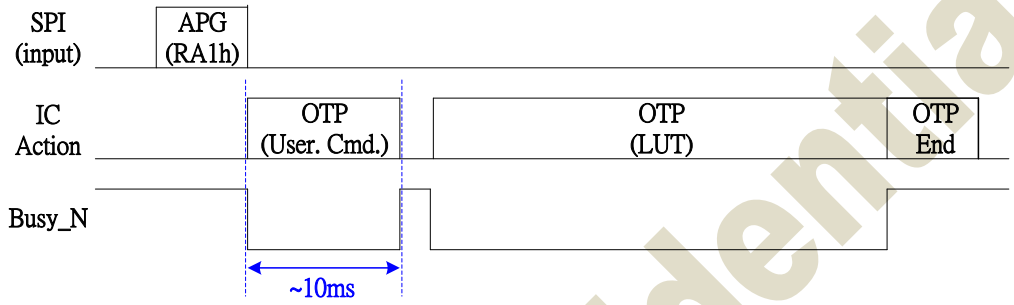
1.Default setting 內 0x020 OTP data 需設定為 A5

2.OTP 0x048 燒入值會依照 register cmd.(RF1h)下 code 值來做燒入

3.上表 value 為 default 值，initial code 有調整時，需依照實際填寫的值來填入

4.3 BUSY_N flag of OTP Program

RA1h 燒錄的期間，OTP 會分成兩部份(user cmd. & LUT)去燒錄，所以 busy_n 會分兩次拉 low，建議下 APG(RA1h) cmd.後，**delay 20ms** 再做 busy_n 拉 high 的偵測，來確定是否燒錄完成。



5. REVISION HISTORY

Revision	Content	Date
1.0	New Issue	2020/07/02
1.1	New Issue	2021/03/24
1.2	1. Initial code modify(P10~P11) 2. IC vender ID modify(P60)	2021/11/11